Paper

Highly-Efficient Low-Voltage-Operation Charge Pump Circuits Using Bootstrapped Gate Transfer Switches

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This paper describes highly efficient on-chip high-voltage multipliers using charge pump circuits. The proposed charge pump circuits use bootstrapped gate transfer switches to avoid the threshold voltage drop in conventional Dickson charge pump circuits and enables them to generate a given voltage with a smaller number of pumping stages, which results in higher efficiency. The SPICE simulation results show that the proposed circuits have high pumping gain, are suitable for low-voltage operation, and have ample current drive capability.

Keywords: Voltage Multiplier, Charge Pump, High Voltage Generator, Bootstrap Circuit

1. Introduction

Charge pump circuits generate higher output voltages than the regular supply voltage, and they have been used in non-volatile memories - such as EEPROM and flash memories - for programming and erase operations through their floating gates. They are also used for low-supply-voltage switched-capacitor systems that require high voltages to drive analog devices. Most MOS charge pump circuits are based on Dickson [1], and Fig.1 shows a four-stage Dickson charge pump circuit. The drain-gate connected NMOS FETs (MD1 - MD5) here are used as diodes, so charge can be pumped in only one direction. CLK and $\overline{CLK}$ are two out-of-phase pumping clocks, whose amplitude is usually the supply voltage V_{dd}, and C_1 - C_4 are coupling capacitors with the same capacitance, C. The two clocks push the charge upward through the MOSFETs, and hence increase the node voltage. The voltage fluctuation ΔV at each node is given by

$$\Delta V = V_\phi \frac{C}{C + C_s} - \frac{I_{out}}{f(C + C_s)} \quad \cdots\cdots\cdots\cdots (1)$$

where C_s is the stray capacitance at each node, I_{out} is the output current loading, f is the frequency of the pumping clocks, and V_ϕ is the effective amplitude of the clock signal [5].

When CLK goes from high to low and $\overline{CLK}$ from low to high, the voltage at node 1 settles to $V_1 + \Delta V$, and the voltage at node 2 to V_2, where V_1 and V_2 are defined as the steady-state lower voltage at nodes 1 and 2 respectively. Both MD1 and MD3 are reverse biased, the charges are pushed from node 1 to node 2 through MD2, and the final voltage difference between nodes 1 and 2 is the threshold voltage of MD2. Hence the necessary condition for the charge pump to work is

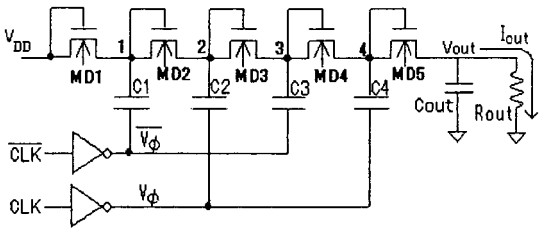

Fig. 1. Four-stage Dickson charge pump.

$$\Delta V > V_{th} \quad \cdots\cdots\cdots\cdots (2)$$

and the voltage pumping gain for the second pumping stage can be defined as

$$G_{V_2} = V_2 - V_1 = \Delta V - V_{th}(V_2) \quad \cdots\cdots\cdots\cdots (3)$$

where $V_{th}(V_2)$ is the threshold voltage of MD2, modified by the body effect due to the source voltage V_2. Then the output voltage of an n-stage charge pump circuit, V_{out}, can be obtained by

$$V_{out} = V_{dd} + n\Delta V - \sum_{k=1}^{n} V_{th}(V_k). \quad \cdots\cdots\cdots\cdots (4)$$

However we can observe that this charge pump has the following drawback; the threshold voltage drop of MD1-MD5 causes a drop in the output voltage V_{out} of $\sum_{k=1}^{n} V_{th}(V_k)$. In other words, the pumping gain for k-th stage is degraded by $V_{th}(V_k), (k = 1, 2, ..., n + 1)$.

Note that for a given output current I_{out}, the total input current I_{in} provided from V_{dd} through the clock drivers to the charge pump circuit is given by

$$I_{in} = (n+1)I_{out} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (5)$$

where parasitic capacitances are neglected for simple explanation of the principle. Since the efficiency η is given by

$$\eta = \frac{V_{out}I_{out}}{V_{dd}I_{in}}, \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (6)$$

we see that as the number of stages, n, increases, the input current I_{in} increases and hence the efficiency drops. Our proposed charge pump circuits presented in the following sections overcome this problem by employing bootstrapped gate transfer switches, and thus they have the following advantages:

- **High Efficiency** : the output voltage of the proposed circuits is given by

$$V_{out} = V_{dd} + n\Delta V \quad \cdots\cdots\cdots\cdots\cdots\cdots (7)$$

  and hence for a specified output voltage, the proposed circuits require a smaller number of stages than conventional circuits, which results in higher efficiency.
- **Low Voltage Operation** : The condition of Eq.(2) does not apply to the proposed circuit, and hence it can operate with low supply voltage.

Remark : (i) According to eq.(5), the total input current I_{in} from V_{dd} is determined by the output current I_{out} and the number of stages n, and it does not depend on the clock frequency f.
(ii) It follows from eqs.(1), (4) and (6) that the efficiency of the circuit drops when we decrease the frequency f to adjust the output voltage V_{out}.
(iii) The on-resistance of the MOS transfer switches must be sufficiently small for eq.(7) to be valid, and this restriction is discussed in the Appendix.

2. Proposed Charge Pump Circuits

In this section we propose two charge pump circuits which use bootstrapped gate transfer switches [2] [3] to improve the efficiency and enable low voltage operation.

A. CMOS Process : Hereafter we consider to use an *N-well* CMOS process, which is suitable for generating high *positive* voltages because the body voltage of PMOS is controllable. On the other hand, a *P-well* process is suitable for generating *negative* voltages, and the *triple-well* process is more flexible than both the above but it is costly.

B. Proposed Circuit 1 : Fig.2 (a) shows our first proposed charge pump circuit, four stages. (Of course, extension to general n-stage is straightforward.) The key features of its operation are as follows:

- OFF state: When the voltage at node D is low, a capacitor C_B is charged to C_BV_{dd}, while the gate of the NMOS switch M is connected to ground and hence M is OFF (Fig.2 (c)).
- ON state: When the voltage at node D is high, the

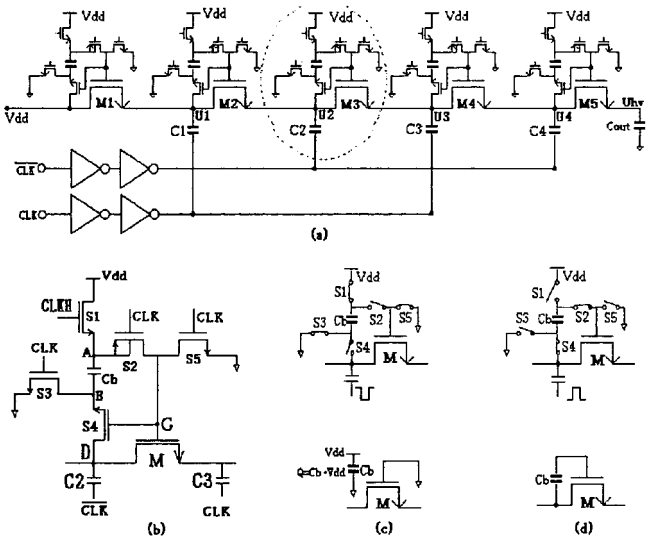

Fig. 2. The first proposed charge pump circuit. (a) Whole circuit (four-stage case). (b) Bootstrapped gate transfer switch. (c) OFF state. (d) ON state.

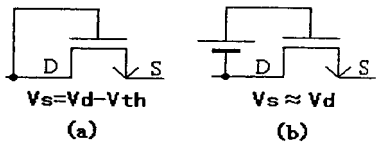

Fig. 3. Transfer switch in ON state. (a) Dickson charge pump circuit. (b) Proposed charge pump circuit.

drain-gate voltage of M is V_{dd} by connecting the drain and gate of M across C_B and hence M is ON (Fig.2 (d)).

Since the drain-gate voltage of M is V_{dd} during ON state, the voltage drop between the drain and source is close to zero in steady state (Fig.3 (b)) so that the threshold voltage drop problem in the conventional Dickson charge pump (where the voltage drop between the drain and source is V_{th} in steady state as shown in Fig.3 (a)) is overcome. In addition, the finite ON-resistance of M in the proposed configuration (Fig.3(a)) is much smaller than that in diode-connected MOS switch (Fig.3(a)); for a square-law NMOS device that operates in the triode region, its ON-resistance R_{on} is given by

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{th})}, \quad \cdots\cdots\cdots\cdots\cdots (8)$$

where μ_n is the electron mobility, W is the channel width, L is the channel length, C_{ox} is the gate oxide capacitance per unit area, V_{gs} is the gate-source voltage and V_{th} is the threshold voltage. Since V_{gd} is equal to V_{dd} and hence V_{gs} is larger than V_{dd} in Fig.3 (b), R_{on} is smaller than that in Fig.3 (a) and a larger current can flow through M with the same device size of W/L. (See Appendix for the effectiveness of small R_{on}.)

Fig.2 (b) shows the circuit implementation of the above, and noting that the voltage of each node can be higher than V_{dd}, the key features of the implementation are given as follows:

- During OFF state, $S1, S3$ and $S5$ are ON while $S2$ and $S4$ are OFF. During ON state, $S2$ and $S4$ are ON while $S1, S3$ and $S5$ are OFF.
- The switch $S1$ is realized with an NMOS device instead of a PMOS device; if it is realized with a PMOS device, it may not turn off even when its gate voltage is V_{dd} because the voltage of node A can be higher than V_{dd}. Note that since the switch $S1$ is realized with an NMOS device, the control voltage (gate voltage) to turn on $S1$ is $2V_{dd}$ produced by a $2V_{dd}$ generator in Fig.4 [4]; if V_{dd} is used instead of $2V_{dd}$ to turn on $S1$, V_{gs} of the sampling switch in track mode is equal to $V_{dd} - V_{th}$ instead of V_{dd}.
- The body of the PMOS switch $S2$ is connected to node A, because the voltage of node A is always higher than that of node B.
- Note that the gate of NMOS switch $S4$ is connected to node G. During ON state, CLK is low and the gate voltage of $S4$ is higher than the voltage at node B by V_{dd}, and hence $S4$ is ON. On the other hand, during OFF state, CLK is high and the gate voltage of $S4$ is zero, and hence $S4$ is OFF.

C. Proposed Circuit 2 : In our first proposed circuit of Fig.2, the size of the NMOS M is much larger than other switch MOSFETs so that its gate capacitance (C_{gs} and C_{gd}) are relatively large and the dynamic power dissipation due to charge/discharge to the gate capacitance is not negligible. During ON state, the voltage of node G is high and the parasitic capacitors associated with node G are charged, while during OFF state the gate of NMOS switch M is connected to ground, and the charge of the parasitic capacitors is discharged. From a power dissipation viewpoint, the discharging of this charge is a waste of energy, and reduces the potential pumping gain.

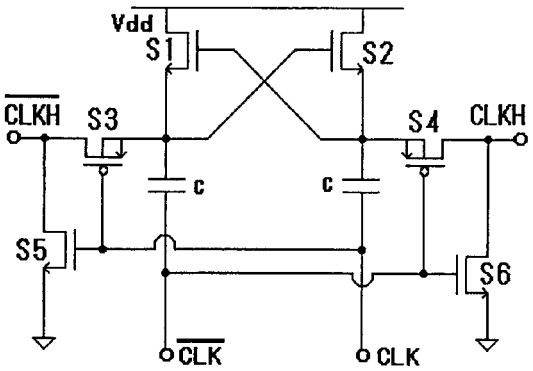

Fig. 4. 2 V_{dd} clock generator [4].

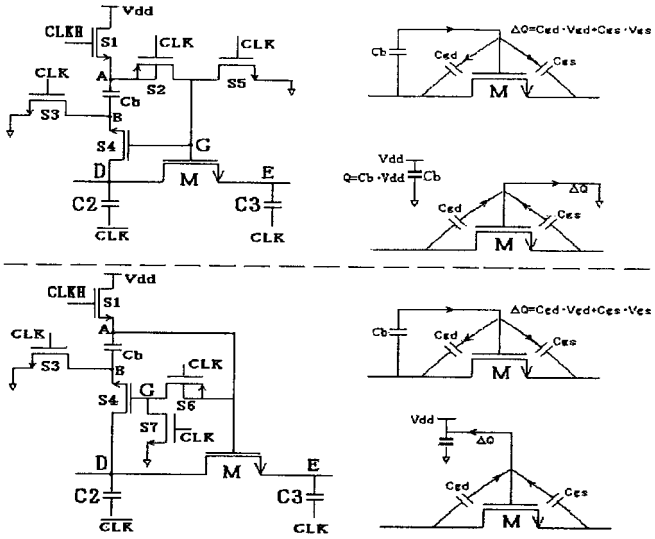

Fig. 5. The second proposed charge pump circuit.

We propose the improved circuit shown in Fig.5, where the gate of the NMOS switch M is connected to node A. During ON state, $S6$ and $S4$ are ON while $S1, S3$ and $S7$ are OFF, and C_{gs}, C_{gd} of M are charged. During OFF state, $S6$ and $S4$ are OFF while $S1, S3$ and $S7$ are ON, and remark that the charges of C_{gs} and C_{gd} are injected back to C_B but not to ground because the gate of NMOS switch M is connected to node A so that the charge is not wasted. Note that during OFF state, the gate voltage of M is V_{dd} but M can be off because the voltages at nodes D and E are equal to or higher than V_{dd}.

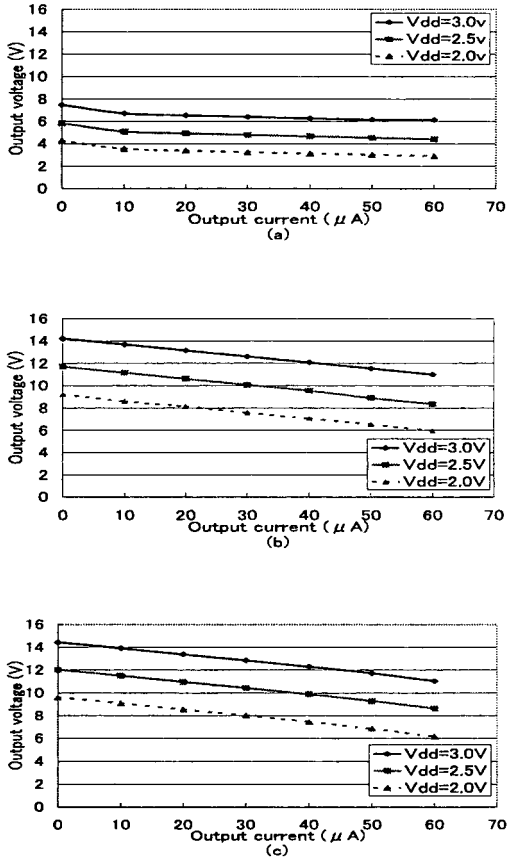

Fig. 6. SPICE simulation result comparison of V_{out} vs. I_{out} characteristics of the conventional Dickson charge pump circuit (Fig.1), our first proposed circuit (Fig.2) and our second proposed circuit (Fig.3) with four stages, C of $15pF$, C_{out} of $30pF$, f of $5MHz$ and V_{dd} of 2.0V, 2.5V and 3.0V. (a) The conventional Dickson charge pump circuit. (b) The first proposed circuit. (c) The second proposed circuit.

3. SPICE Simulation Results

Fig.6 shows a SPICE simulation result comparison of V_{out} vs. I_{out} characteristics of the conventional Dickson charge pump circuit, our first proposed circuit and our second proposed circuit with four stages, C of $15pF$, C_{out} of $30pF$, f of $5MHz$ and V_{dd} of 2.0V, 2.5V and 3.0V. We see that the second proposed circuit achieves the highest output voltage among them. (e.g., for V_{dd}=3.0V and $I_{out} = 20\mu$A, the output voltage of Dickson charge pump is 6.5V, that of the first proposed circuit is 13.1V while that of the second proposed circuit is 13.4V).

Fig.7 compares SPICE simulations of *Efficiency* vs. I_{out} characteristics for the conventional Dickson charge pump circuit, our first proposed circuit and our second proposed circuit with four stages, C of $15pF$, C_{out} of $30pF$, f of $5MHz$, and V_{dd} of 2.0V, 2.5V and 3.0V. We see that the second proposed circuit achieves the highest efficiency of the three (e.g., for V_{dd}=3.0V and $I_{out} = 20\mu A$, the efficiency of Dickson charge pump is 43.6%, that of the first proposed circuit is 87.7% while that of the second proposed circuit is 89.2%).

Fig.8 compares SPICE simulations of V_{out} vs. I_{out} characteristics for the conventional Dickson charge pump circuit, our first proposed circuit and our second proposed circuit with the clock frequency varied from f to $4MHz$, $5MHz$, $6MHz$, $8MHz$ and $10MHz$, and with four stages, C of $15pF$, C_{out} of $30pF$, and V_{dd} of 3.0V. We see that for each circuit, V_{out} increases as f increases, which can be explained by eq.(1), and that the second proposed circuit achieves the highest output voltage of the three for each frequency. (e.g., for V_{dd}=3.0V, $I_{out} = 20\mu$A and f=10MHz, the output voltage of Dickson charge pump is 6.6V, that of the first proposed circuit is 13.7V while that of the second proposed circuit is 13.9V).

4. Concluding Remarks

- Fig.6 (b) and (c) show that the output voltages V_{out} of the first and second proposed circuits can not achieve $5V_{dd}$ even when the output current I_{out} is equal to 0. This is mainly because the capacitor C_B for the bootstrap works as a part of parasitic capacitances C_s in eq.(1). The voltage at node A in the upper part of Fig.5 (the first proposed circuit) goes to zero when the transmission gate M is off, while the voltage at node A in the lower part of Fig.5 (the second proposed circuit) is V_{dd} when M is off. Hence the charge stolen from node D to the capacitor C_B in the first proposed circuit is smaller than that in the second one when the MOS switch $S4$ turns on, and then the second proposed circuit achieves the higher output voltage.
- In other words, the second proposed charge pump circuit has two advantages over the first proposed one.
  (1) The dynamic power dissipation due to charge/discharge to the gate capacitance of transfer switches is reduced.

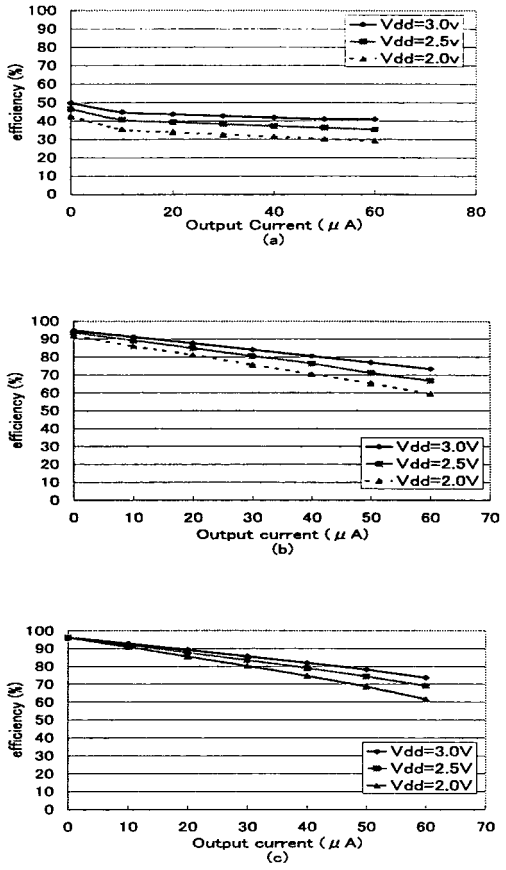

Fig. 7. SPICE simulation result comparison of *Efficiency* vs. I_{out} characteristics of the conventional Dickson charge pump circuit (Fig.1), our first proposed circuit (Fig.2) and our second proposed circuit (Fig.3) with four-stage, C of $15pF$, C_{out} of $30pF$, f of $5MHz$. and V_{dd} of 2.0V, 2.5V and 3.0V. (a) The conventional Dickson charge pump circuit. (b) The first proposed circuit. (c) The second proposed circuit.

(2) The effect of capacitor C_B for the bootstrap on pump gain reduction is alleviated.

- The body of each transfer switch NMOS in our proposed circuits as well as Dickson charge pump circuit is connected to ground and its threshold suffers from body effect [6]. Note especially that the body effect is most severe at the output node; in Fig.2, the body effect of M4 is larger than that of M2, or in other words, the threshold voltage of M4 is larger than that of M2. In Dickson charge pump, the increase of the threshold voltage due to the body effect degrades the output voltage (see Eq.(4)), and thus it degrades the efficiency η which is given by

$$\eta = \frac{V_{dd} + n\Delta V - \sum_{k=1}^{n} V_{th}(V_k)}{(n+1)V_{dd}}. \quad \cdots\cdots (9)$$

  In our proposed circuits, there is no output voltage drop due to the threshold voltage and our proposed circuits are much more tolerant of body effect than the Dickson charge pump circuit. However note that the body effect increases the ON-resistance of the transfer switch given by Eq.(8), and hence it degrades the performance. Furthermore, if the threshold voltage becomes larger than V_{gs} due to body effect, the circuit does not function as a charge pump.
- If we use a *triple-well* process, the body voltage of the transfer switch is controllable and some circuit techniques may avoid the body effect [7]. However the control of the body may cause latch up, and experimental verification that there is no latch-up would be required even if the circuit works in SPICE simulations, and also the triple-well process is costly.
- Recently several other charge pump configurations, with the gate of the transfer switch boosted, have been proposed [5] [7] [8], and the major advantage of our proposed circuits over these is that the gate of the transfer switch at the output node can be boosted, while in the other configurations it is difficult.

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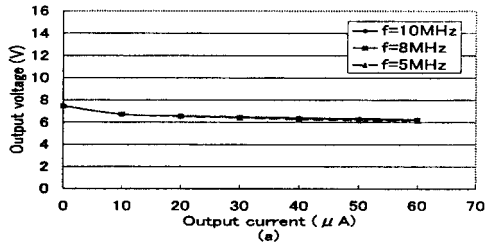

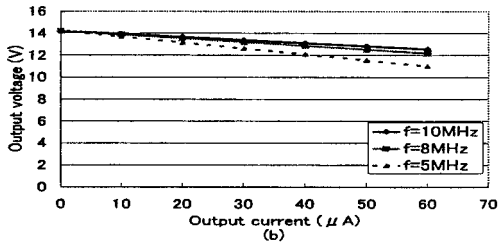

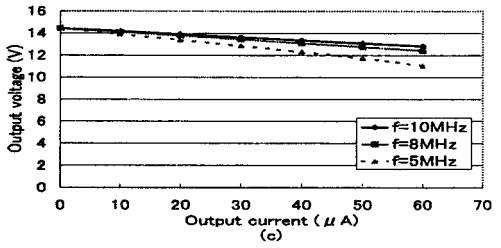

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Appendix

1. Effect of ON-Resistance of MOS Transfer Switch

This appendix shows that the ON-resistance of MOS transfer switches, given by eq.(8), must be sufficiently small in order for eq.(7) to be valid. Letting the second term of the right-hand in eq.(1) be

$$dv = \frac{I_{out}T}{(C + C_s)} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \text{(A1)}$$

where $T(= 1/f)$ is a clock period, and then the current $i(t)$ which flows through the MOS transfer switch in ON-state is given by

$$i(t) = \frac{dv}{R_{on}} \exp(-\frac{t}{(C + C_s)R_{on}}). \quad \cdots\cdots\cdots \text{(A2)}$$

In order for eq.(7) to be valid, the drain-source voltage of the MOS transfer switch in ON-state must be almost zero at the end of ON-state; in other words, if the clock duty is 50% (the MOS transfer switch is ON during $T/2$ while it is OFF during the other $T/2$), the following has to be satisfied:

$$i(\frac{T}{2}) \approx 0. \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \text{(A3)}$$

Then we see that R_{on} has to be small enough for given C, C_s, I_{out} and T, and we can perform quantitative calculation using eqs. (A1), (A2) and (A3). Our proposed charge pump circuits make R_{on} smaller by bootstapping the gate voltage which helps satisfy eq.(A3).

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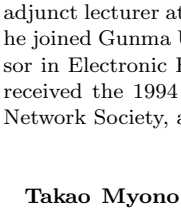

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