Paper

Multiple-height Microstructures Fabricated by ICP-RIE and Embedded Masking Layers

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Due to the processing limitation of photolithography, only width and length have been controllable parameters for designing mechanical characteristics of silicon micromachined structures, while thickness has been left pre-determined by the thickness of layers. The range of electromechanical properties have been, therefore, strongly limited by the practical range of these tunable parameters. In this paper, we present a universally applicable fabrication technique to realize multiple-height microstructures by locally controlling the etching depth of ICP-RIE (inductively coupled plasma - reactive ion etching). Several layers of etching masks of different materials have been prepared on the initial surface of substrate to avoid repeating photolithography on the etched surfaces. This technique enables us to have one more degree of freedom in designing MEMS structures.

Keywords: ICP-RIE, multi-height structure, MEMS, HARMS

1. Introduction

Controlling the structural height as well as the width and length of MEMS (micro electro mechanical system) structures becomes inevitable for extending designing range of mechanical characteristics. While conventional bulk micromachining only enables us to design under limitations such as crystallographic orientation and practical range of etching rate, combining different types of fabrication process has been used to relax such regulations: for instance, LIGA process [(1)], wafer bonding [(2)] and multi-level surface micromachining [(3)]. Most of these, however, require expensive equipments or extra processing steps.

DRIE (deep reactive ion etching) is commonly used to make HARMS (High-Aspect Ratio Micro Structure). Structures whose thickness is locally tailored, however, have not been realized easily, because photolithography is difficult after DRIE in presense of deep etched steps. Therefore, a new manufacturing method of the multi-step structure has been developed by using isotropic etching by XeF_2 after dry etching [(4)]. Some groups have proposed batch processes to fabricate multiple-height HARMS by using ICP-RIE (Inductively Coupled Plasma Reactive Ion Etching) of silicon, which requires only planar lithography on the initial surface of the substrate [(5)~(9)]. In this paper, we generalize such fabrication technique to DMP (Delay-Masking Process), and demonstrate straightforward processes of making silicon and organic-material structures of multiple steps.

2. Process Flow of DMP

One of the variations of DMP is illustrated in Fig. 1. In step (a) to (c), etching masks of different materials (namely, silicon oxide and photoresist), which have etching-selectivity, are deposited on a silicon substrate. In step (d), the wafer is etched by deep RIE using the upper-most layer of masks. We used ICP-RIE by conditioning the processing recipe [(10)]. Next in step (e), the upper-most etching mask is selectively stripped, and the second deep RIE step is performed using the second masking layer (silicon oxide). Multiple-height structure is thus made by repeating etching of silicon and removing masking layers.

The process is to make a particular structure shown in Fig. 2. Generalized fabrication technique will be discussed later.

3. Fabrication Result

SEM (Scanning Electron Microscope) micrographs of fabricated structure (top and bottom surfaces) are shown in Fig. 2. A multiple-height structure with vertical walls of high aspect ratio (up to 20) was successfully obtained by this newly developed DMP. The angle of vertical wall to the surface was measured to be 85±4 degrees.

In the first ICP-RIE step, trenches of 100μm deep were formed. After photoresist removal and cleaning, the sample was etched another 50μm deep by second ICP-RIE step. Thanks to the anisotropic etching of DRIE, the profile of the first trench etching is preserved in the subsequent etching steps. Thus it was possible to make fine and complicated structures without causing alignment error between the etching masks.

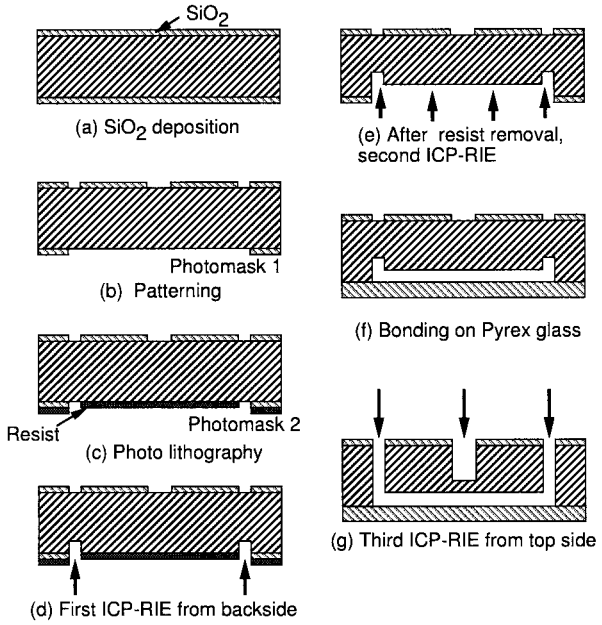
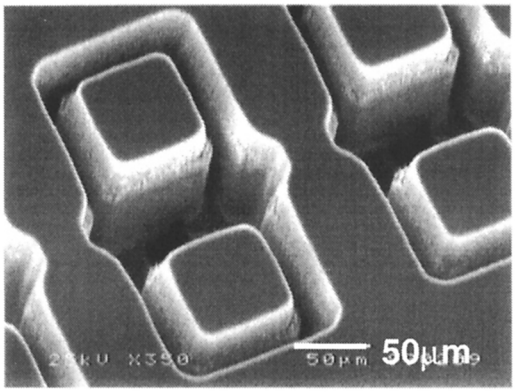
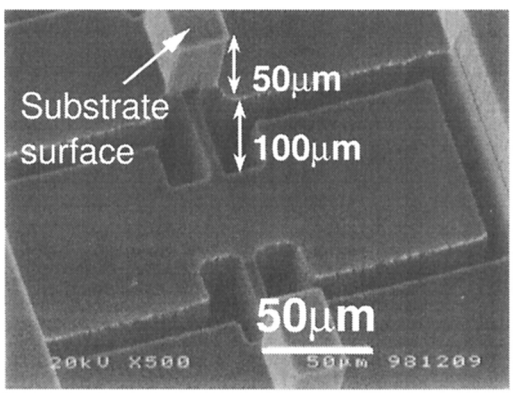


Fig. 1. Process Flow

(a) LPCVD of silicon dioxide deposition on silicon substrate. (b) Patterning of the silicon dioxide by using photomask-1. (c) Photolithograph on the backside by using photomask-2. (d) Trench etching by ICP-RIE from backside by using the photoresist mask. (e) After stripping the resist, ICP-RIE from backside by using silicon dioxide mask. (f) Wafer bonding onto a Pyrex glass. (g) front side ICP-RIE for separation.



(a) Front view of the sample



(b) Delay-masking process for multi-height structure

Fig. 2. SEM view

4. Triple DMP

Three-level HARMS could be fabricated by the same process. Silicon dioxide, aluminum, and photoresist are use for masking layers for triple DMP. Figure 3 shows process flow of the triple DMP. First, silicon dioxide layer was deposited by LPCVD (Low Pressure Chemical Vapor Deposition) on a silicon substrate. After patterning the layer by photomask-1, aluminum layer was deposited by vacuum evaporation and patterned by photomask-2. The substrate was then coated with photoresist and lithographed by photomask-3. Having prepared the masks, we etched the front surface of the silicon substrate by ICP-RIE by using the photoresist mask. After stripping the photoresist by O_2 ashing, the surface was patterned by ICP-RIE again by using the embedded aluminum mask. Finally, after removing the aluminum and cleaning the substrate by H_2SO_4+H_2O_2, final ICP-RIE was processed on the front side of the substrate by using the silicon dioxide mask, which had been prepared at the beginning of the process.

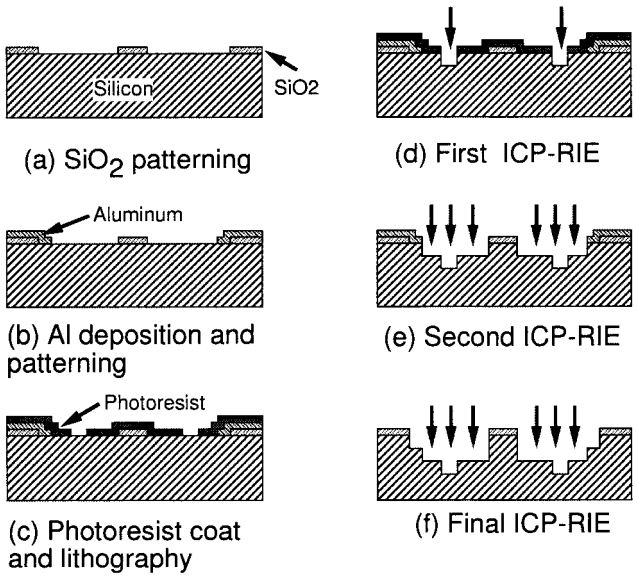


Fig. 3. Process Flow of triple DMP

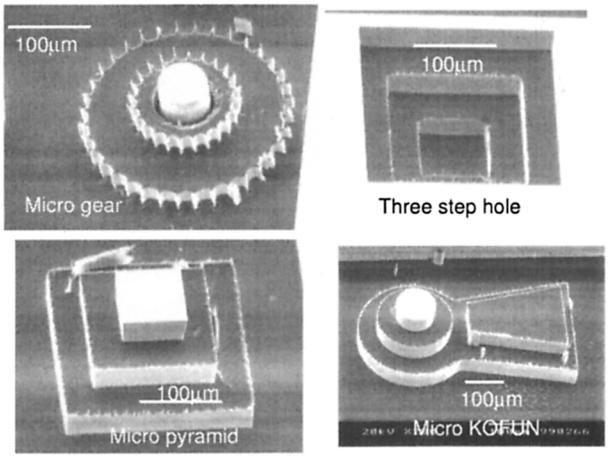


Fig. 4. SEM view of three level structure

Figure 4 shows triple DMPed structures. Three level structures were made by repeating the DMP tree times.

We occasionally found protrusions extending on the edge of the vertical wall, which are silicon-based by-product of ICP-RIE. These can be removed by isotropic dry etching of silicon by using SF_6.

5. Combination of DMP and Wafer Bonding

Wafer bonding of glass and silicon are usually used to produce mechanically movable microstructures. One approach may be preparing a dimple on a glass substrate to be aligned to free-standing part on a silicon substrate, which occasionally leads to misalignment of wafers. Here, we propose alternative simple approach of wafer bonding to obtain equivalent results, assisted by DMP to eliminate the alignment problem.

First in Fig. 5(a), silicon dioxide and photoresist masks are prepared. (b) Backside of the silicon is processed by ICP-RIE to make release trenches, (c) and then a Pyrex glass is bonded. (d) ICP-RIE is performed on the front side makes deep trenches in silicon. (e) After photoresist removal, the front side is etched by ICP-RIE again to release the microstructures. Finally in (f), silicon dioxide is removed, and the whole area is covered by bonding another Pyrex glass. Note that no glass etching is needed in this process.

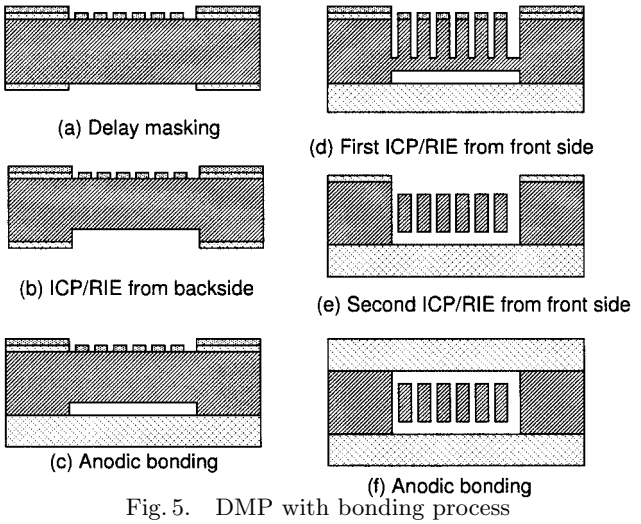


Fig. 5. DMP with bonding process

6. DMP of organic material

DMP is also applicable to organic materials such as photoresist and PMMA; there are usual used as a mold for electroplating. Although multiple-height structures are formed by LIGA or other UV lithography, they require several steps of high-energy exposures and surface planarization processes. On the other hand, we present using DMP for organic materials patterned into equivalent molding structures by simplified processing steps.

Fig. 6 shows process flow of the organic DMP. First in step (a), photoresist or PMMA was spun on a silicon substrate. After First mask(SiO_2) was deposited on the photoresist or PMMA by sputter and patterning of the first mask, the second mask (silicon) was deposited by sputter and patterned. After first O_2 plasma ashing of photoresist by 20μm deep, the silicon mask was removed by RIE and followed by the second O_2 plasma ashing by 10μm deep. Finally, SiO_2 mask was removed by HF. SEM view of DMP on photoresist is shown in Fig. 7.

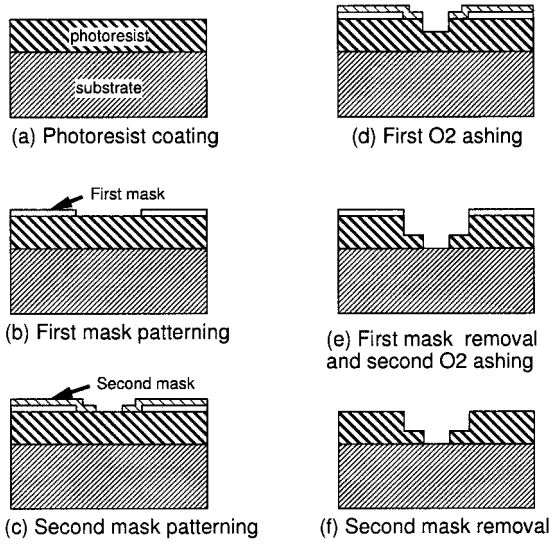


Fig. 6. Organic DMP

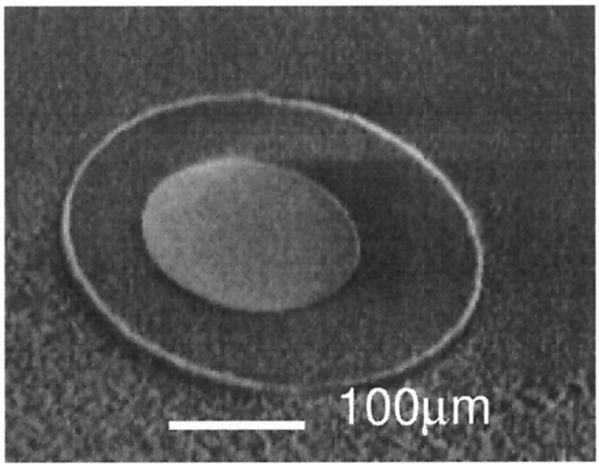


Fig. 7. SEM view of Organic DMP

7. Discussions

For successful result of this process, one needs to clean the wafer after each removal of masking layer in order to avoid micro-mask effect (See Fig. 8).

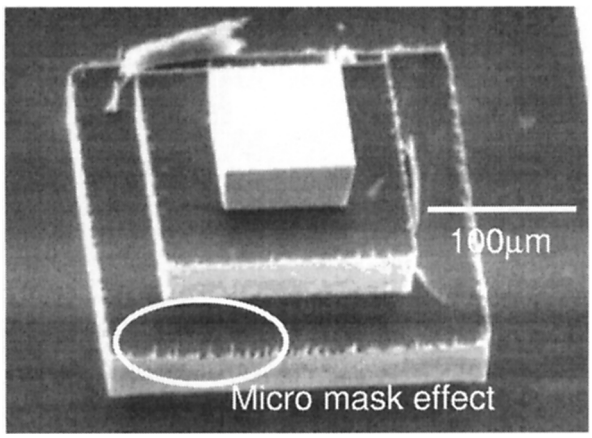


Fig. 8. SEM view of micro mask

Selections of materials for those masking layers are also essential to optimize the fabrication process. Table 1 shows etching selectivity of several materials. For

three-step DMP, we used silicon dioxide, aluminum and posi-photoresist for masking layers. Posi-photoresist was removed by O_2 ashing, while aluminum and SiO_2 were not preserved. Aluminum etchant can only remove aluminum. For DMP of more steps, our group newly developed Al-DMP [11] which uses combination of layered photoresist and aluminum only. In this process, photoresist protects underlying aluminum layers when stripping the top layer of aluminum mask by wet etching. Etching rate depends on the location on a wafer due to the loading effect of RIE. Thus one may also need to carefully control the etching rate by observing etching depth time to time.

Material	Acetone	O_2 ashing	Al etchant	HF
Posi-photoresist	x	x	o	o
Nega-photoresist	o	x	o	o
Aluminum	o	o	x	x
SiO_2	o	o	o	x

Table 1. Etching selectivity of materials. x-attacked o-OK

8. Conclusions

We have developed a new process to produce microstructures of multiple heights by using etching selectivity of two or more masking layers. Several masking layers have been prepared at the beginning of the process, and silicon microstructures of plural etching depths can be fabricated by ICP-RIE by stripping the mask layer by layer. Since these masking layers are photolithographically defined on the initial planar surface of the substrate, fine dimensional control is possible with minimal alignment error. Three variations of delay-masking process (DMP) have been proposed: DMP for two- or three-step structures with two or three embedded masks, respectively, and DMP for organic materials. The number of steps is not limited to these numbers. The process presented here has compatibility with post-processing of silicon substrate after CMOS processes.

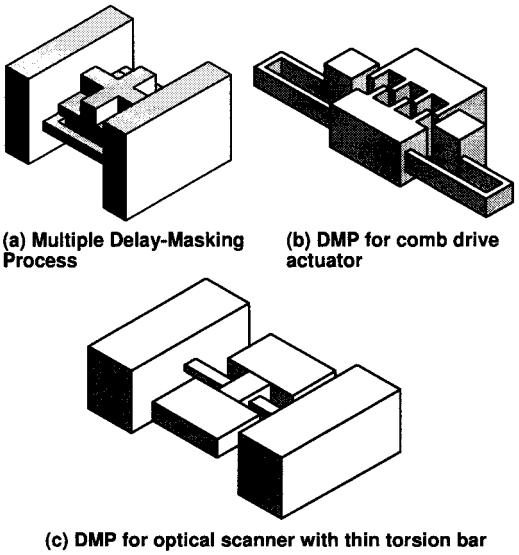


Fig. 9. Example of 3-D structure by multiple DMP

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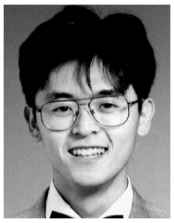

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