Paper

Design of a fuzzy based circular pattern recognition circuit using current-mode techniques

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A fuzzy based circuit to recognize circular patterns is proposed in this paper. The proposed algorithm calculates the center coordinates of the target patterns. The simple algorithm and exemption from the use of template patterns as well as multipliers enable the proposed circuit to implement on the hardware of an economical scale. Furthermore, the circuit design by using current-mode techniques provides easy extendability of the circuit and efficient pattern recognition with high-speed. The validity of the proposed algorithm and the circuit design is confirmed by computer simulations. The proposed pattern recognition circuit is integrable by a standard CMOS technology.

Keywords: pattern recognition systems, current-mode circuits, fuzzy systems, noise elimination systems, image processing

1. Introduction

Recently, necessity for intelligent support systems [1]-[4] is increasing in the field of the primary industry because of the decrease in the working population. For example, the intelligent support systems to harvest fruits instead of human being are required in the field of agriculture. Among others, in Kumamoto which is a special production localities of water melons, the harvest of the water melon imposes on the harvesters the serious burden of carrying heavy products.

To harvest fruits by using intelligent support systems, the design of the pattern recognition system which is a building block of the support system to calculate the coordinates of the target objects is important. For this reason, several methods have already been proposed for the realization of the pattern recognition systems [5]-[10]. Among others, template matching [6]-[10] is the most famous method in the pattern recognition problem. The disadvantages of this method are requirement of large number of the template patterns and large computational time which depends on the size of the input image. Furthermore, most of the pattern recognition systems using template matching are realized by using software systems on digital computers or voltage-mode circuit designed by using HDL (Hardware Description Language) [11] since the algorithm of the template matching is very complex [8]-[10]. Therefore, they require a higher speed microprocessor and larger capacity memories. To realize the real-time processing and the economical hardware scale for the pattern recognition systems, the simple algorithm and architecture are required.

In this paper, a fuzzy based circuit to recognize circular patterns such as water melon, orange, etc. is proposed. The proposed algorithm calculates the center coordinates of the target patterns. The simple algorithm and exemption from the use of template patterns as well as multipliers enable the proposed circuit to implement on the hardware of an economical scale. Furthermore, the circuit design by using current-mode techniques [12],[13] provides easy extendability of the circuit and efficient pattern recognition with high-speed. The validity of the proposed algorithm and the circuit design is confirmed by computer simulations. Concerning 16×16-pixel and 8×8-pixel binary images, the performance of the proposed circuit is analyzed by SPICE [14] simulations.

2. Architecture

Figure 1 shows the architecture of the proposed pattern recognition circuit. The proposed circuit consists of $m \times n$ cells. In Fig.1, (i, j) denotes the coordinates of the cells. As an input to the proposed circuit, the $m \times n$-pixel binary image is given. The pixels of the input image correspond to the coordinates of the cells.

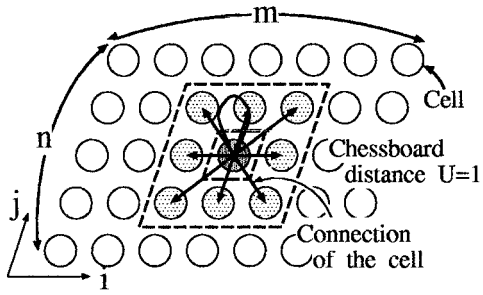

Fig.1 Architecture of the proposed pattern recognition circuit.

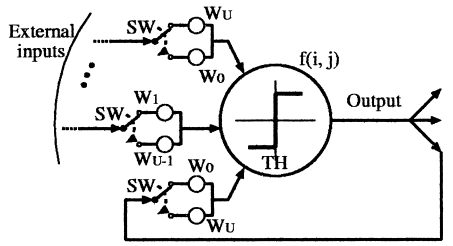

Fig.2 Block diagram of the cell for the proposed circuit.

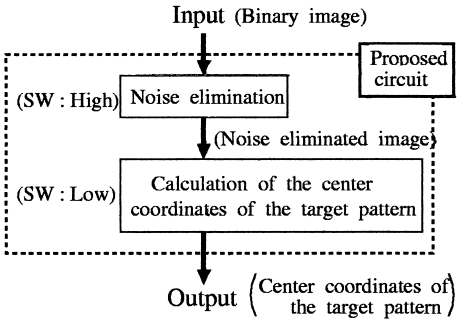

Fig.3 Flow of the circular pattern recognition.

Figure 2 shows the block diagram of the cell for the proposed circuit. In Fig.2, the output function of the cell is a unit-step function. The threshold value of the unit-step function is denoted by TH. In Fig.2, the cell $f(i,j)$ is connected to the cell which are located within a chessboard distance U (see Fig.1). The parameter U is set equal to the radius of the circular pattern. †

Figure 3 shows the flow of the circular pattern recognition. In the proposed circuit, the circular pattern recognition consists of two processes: noise elimination and calculation of the center coordinates of the target pattern. Firstly, the noise elimination is performed for the input image. The proposed circuit is in the noise elimination process when the switches SW's in Fig.2 are in the upper position (see in Fig.3). The connection weights $W_{D((k,l),(i,j))}$'s $(D((k,l),(i,j)) \in \{0,1,\ldots,\mathrm{U}\})$ for the cell $f(k,l)$ are selected by controlling the switches SW's. The connection weights are determined such as the summation of the connection weights for the large cluster becomes larger than that for the small cluster. When the summation of the connection weights for the cell $f(i,j)$ is less than the threshold value TH, the cell $f(i,j)$ is eliminated as a noise.

After the noise elimination finished, the positions of switches are reversed. Then, the proposed circuit calculates the center coordinates of the target pattern. In the calculation of the center coordinartes, the connection weights are determined such as the connection weights from the cell $f(k,l)$ to the cells which located in the distance U become larger than that to the other cells. The cell which has the maximum value of the summation of the connection weights is extracted as center coordinates of the target pattern. When the summation of the connection weights for the cell $f(i,j)$ is larger than the threshold value TH, the cell $f(i,j)$ is extracted as the center coordinates of the target pattern.

The algorithm of the proposed circuit will be given in the following section.

3. Algorithm

The algorithm of the proposed pattern recognition circuit is as follows.

Step1: For the input image, the initial values of the cells, $f^0(i,j)$'s, are set to as follows:

$$f^t(i,j) \in \{0,1\} \qquad (t=0), \quad (1)$$

where 0 and 1 represent the values of the white and black pixels, respectively. In Eq.(1), $f^t(i,j)$ ($i \in \{1,\ldots,m\}$, $j \in \{1,\ldots,n\}$) denotes the value of the (i,j) cell when the time is t.

Step2: By connecting the switches SW's to the upper positions (see in Fig.2), the proposed circuit functions as a noise elimination circuit. For the cell $f^t(k,l)$ ($k \in \{1,\ldots,m\}$, $l \in \{1,\ldots,n\}$) which corresponds to the black pixel, the cells located within a chessboard distance U are weighted. The connection weights $W_{D((k,l),(i,j))}$ $(D((k,l),(i,j)) \in \{0,1,\ldots,\mathrm{U}\})$ are determined by a fuzzification map shown in Fig.4. Here, $D(\cdot)$ denotes the chessboard distance from (k,l) to (i,j). The fuzzification map shown in Fig.4 corresponds to the membership function of fuzzy systems. In the noise elimination process, the connection weights are determined to satisfy the following conditions:

$$\begin{aligned} W_0 &\geq \alpha^{\mathrm{U}} W_{\mathrm{U}}, \\ W_1 &\geq \alpha^{\mathrm{U}-1} W_{\mathrm{U}}, \\ &\cdots \\ W_{\mathrm{U}-1} &\geq \alpha W_{\mathrm{U}}, \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (2) \end{aligned}$$

where α is a positive parameter which satisfies $\alpha > 1$. In case of the noise elimination process, the summation of the connection weights for the cell $f^t(i,j)$, $SP^t_{i,j}$, is given by

$$SP^t_{i,j} = \sum_{\{(i,j)|D((k,l),(i,j))\leq \mathrm{U}\}} f^t(k,l) W_{D((k,l),(i,j))}. \quad \cdots \quad (3)$$

In other words, the Eq.(3) denotes the degree of overlap of the fuzzification maps. Hence, $SP^t_{i,j}$ for a large cluster becomes larger than that for a small cluster.

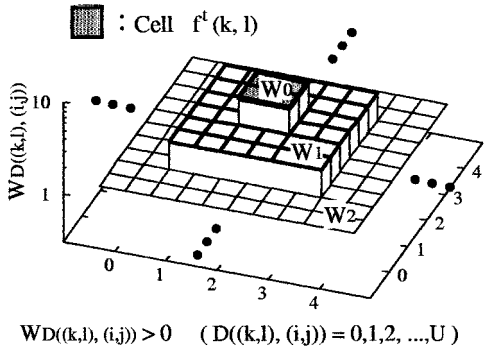

Fig.4 Fuzzification map for the noise elimination process.

†We assume that the radius of the circular pattern can be determined by the kind of a target object and the length of a robot arm used in the intelligent support system.

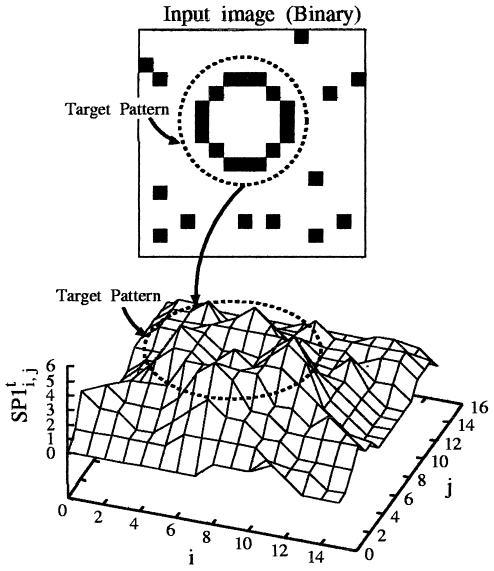

Fig.5 Summation of the connection weights, $SP^t_{i,j}$, for the cell $f^t(i,j)$.

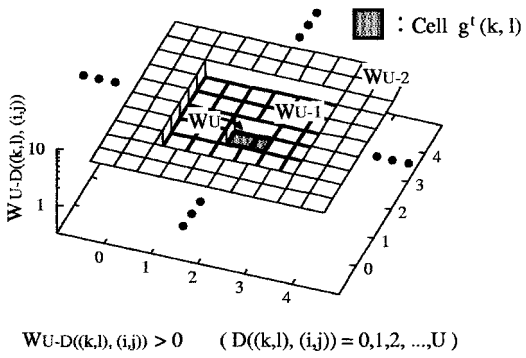

Fig.6 Fuzzification map for the extraction process of the cell which corresponds to the center coordinates of a target pattern.

Figure 5 shows an example of the summation of the connection weights, $SP^t_{i,j}$, for the cell $f^t(i,j)$. As one can see from Fig.5, $SP^t_{i,j}$ for a large cluster is larger than that for a small cluster.

Step3: The noise elimination is performed as follows :

$$g^t(i,j) = \begin{cases} 0 & (SP^t_{i,j} < \mathrm{TH}^t), \\ 1 & (SP^t_{i,j} \geq \mathrm{TH}^t), \end{cases} \quad \cdots (4)$$

where TH^t is the threshold value when the time is t. Thus, the cell $f^t(k,l)$ is extracted as the black pixel when $SP^t_{i,j} \geq \mathrm{TH}^t$. As one can see from Eqs.(3) and (4), the size of the cluster which is eliminated by the proposed algorithm depends on the parameter U. In Eq.(4), the threshold value TH^t is updated as follows:

$$\mathrm{TH}^{t+1} = \mathrm{TH}^t - W_{\mathrm{U}}, \quad \cdots\cdots\cdots\cdots\cdots\cdots (5)$$

where

$$\mathrm{TH}^0 = \mathrm{U}W_0.$$

The noise elimination terminates when the total number of the black pixels, N^t, satisfies $N^{t+1} = N^t$ and $N^t \neq 0$.

Step4: After the noise elimination finished, the positions of switches are reversed. Then, the proposed circuit calculates the center coordinates of the target pattern, $p^t(i,j)$. For the cell $g^t(k,l)$ which is a part of the large cluster, the cells located within a chessboard distance U are weighted. The connection weights $W_{\mathrm{U}-D((k,l),(i,j))}$ $(D((k,l),(i,j)) \in \{0,1,\ldots,\mathrm{U}\})$ are determined by a fuzzification map shown in Fig.6. Hence, the summation of the connection weights for the cell $g^t(i,j)$, $SP^t_{i,j}$, is given by

$$SP^t_{i,j} = \sum_{\{(i,j)|D((k,l),(i,j))\leq \mathrm{U}\}} g^t(k,l) W_{\mathrm{U}-D((k,l),(i,j))}. \quad \cdots (6)$$

From Eq.(6), the summation of the connection weights for the cell $g^t(i,j)$ which corresponds to the center coordinates of the circular pattern becomes larger than that for other cells since the radius of the circular pattern is equal to the parameter U. Figure 7 shows an example of the summation of the connection weights, $SP^t_{i,j}$, for the cell $g^t(i,j)$. As one can see from Fig.7, $SP^t_{i,j}$ for the cell $g^t(i,j)$ which corresponds to the center coordinates of the target pattern is larger than that for other cells.

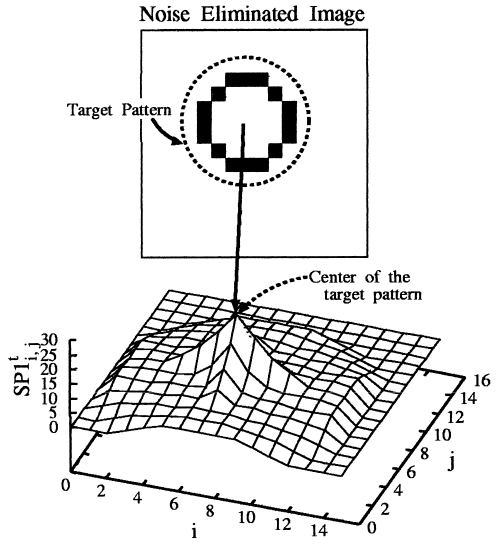

Fig.7 Summation of the connection weights, $SP^t_{i,j}$, for the cell $g^t(i,j)$.

Step5: In the summation of the connection weights obtained by Eq.(6), the cell $g^t(i,j)$ which has the maximum value of $SP^t_{i,j}$ is extracted as center coordinates of the target pattern. The center coordinates of the target pattern is extracted as follows :

$$p^t(i,j) = \begin{cases} 0 & (SP^t_{i,j} < \mathrm{TH}^t), \\ 1 & (SP^t_{i,j} \geq \mathrm{TH}^t). \end{cases} \quad \cdots\cdots (7)$$

Thus, the cell $g^t(i,j)$ is extracted as the center coordinates of the target pattern, $p^t(i,j)$, when $SP^t_{i,j} \geq \mathrm{TH}^t$. In Eq.(7), the threshold value TH^t is updated as follows:

$$\mathrm{TH}^{t+1} = \mathrm{TH}^t - W_{\mathrm{U}}, \quad \cdots\cdots\cdots\cdots\cdots\cdots (8)$$

where

$$\mathrm{TH}^0 = W_0 2\pi\mathrm{U}.$$

The extraction process terminates when the total number of the black pixels, N^t, satisfies $N^t > 0$.

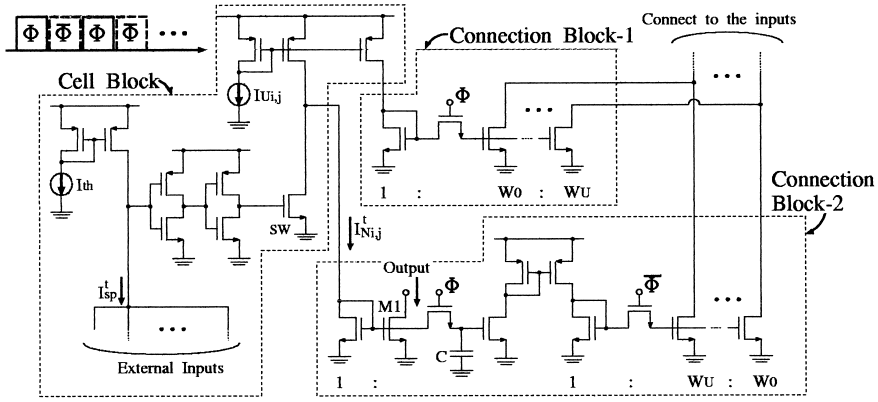

Fig.8 Cell circuit designed by using current-mode techniques.

4. Hardware Implementation

Figure 8 shows the proposed pattern recognition circuit designed by using current-mode techniques. The proposed circuit consists of a cell block and two connection blocks. In Fig.8, the current sources, $\mathrm{I_{th}}$ and $\mathrm{I_{U}}_{i,j}$, correspond to the threshold value TH^t and the pixel value of the input image, $f^t(i,j)$, respectively. The external inputs $\mathrm{I}^t_{\mathrm{sp}}$ corresponds to the summation of the connection weights, $SP^t_{i,j}$.

Firstly, the proposed circuit functions as a noise elimination circuit when the switches ϕ and $\bar{\phi}$ are on and off, respectively. The connection block-1 calculates the summation of the connection weights, $\mathrm{I}^t_{\mathrm{U}i,j} W_{D((k,l),(i,j))}$, for $f^t(i,j)$. In the connection block-1, the connection weights are realized by the ratios of the current mirrors. The ratios of the current mirrors are realized by controlling the channel width of NMOSFET's. The outputs of the connection block-1 are connected to the cell blocks which are located within a chessboard distance U. In the cell block, the summation of the connection weights, $\mathrm{I}^t_{\mathrm{sp}}$, for $f^t(i,j)$ is realized by wired-sum connection. From the output of the connection block-1 the cell block functions as

$$\mathrm{I}^t_{\mathrm{N}i,j} = \begin{cases} 0 & (\mathrm{I_{sp}}^t < \mathrm{I_{th}}), \\ \mathrm{I_{U}}_{i,j} & (\mathrm{I_{sp}}^t \geq \mathrm{I_{th}}), \end{cases} \quad \cdots\cdots\cdots (9)$$

where $\mathrm{I}^t_{\mathrm{N}i,j}$ is the output of the cell block. When the noise elimination process, the output of the cell block, $\mathrm{I}^t_{\mathrm{N}i,j}$, which corresponds to $g^t(i,j)$ can be obtained from the NMOSFET $M1$. The output of the cell block, $\mathrm{I}^t_{\mathrm{N}i,j}$, is stored in the capacitor C.

After the noise elimination finished, the switches ϕ and $\bar{\phi}$ are reversed. Then, the proposed circuit extracts the cell which corresponds to the center coordinates of the circular pattern. The connection block-2 calculates the summation of the connection weights, $\mathrm{I}^t_{\mathrm{N}i,j} W_{\mathrm{U}-D((k,l),(i,j))}$, for $g^t(i,j)$, where $\mathrm{I}^t_{\mathrm{N}i,j}$ is provided from the capacitor C. The outputs of the connection block-2 are connected to the cell blocks which are located within a chessboard distance U. In the cell block, the summation of the connection weights, $\mathrm{I_{sp}}^t$, for $g^t(i,j)$ is realized by wired-sum connection. From the output of the connection block-2 the cell block functions as

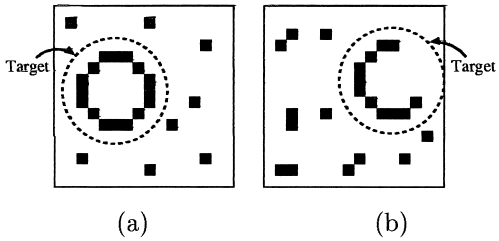

Fig.9 Input images used in numerical simulations. (a) Image-1. (b) Image-2.

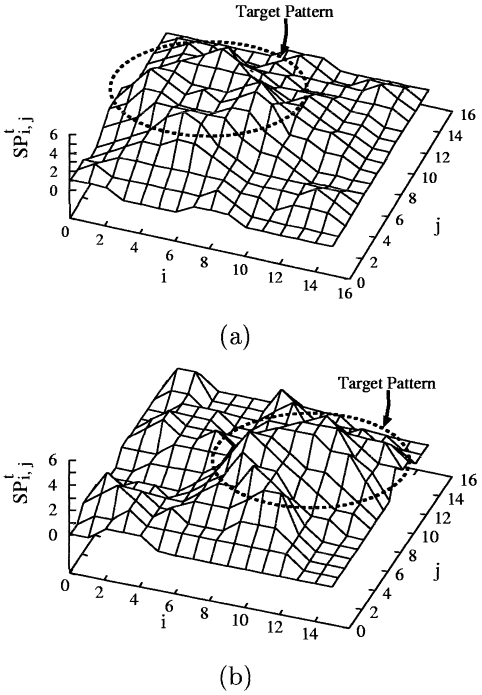

Fig.10 Summation of the connection weights for $f^t(i,j)$. (a) Image-1. (b) Image-2.

$$\mathrm{I}^t_{\mathrm{N}i,j} = \begin{cases} 0 & (\mathrm{I_{sp}}^t < \mathrm{I_{th}}), \\ \mathrm{I_{U}}_{i,j} & (\mathrm{I_{sp}}^t \geq \mathrm{I_{th}}), \end{cases} \quad \cdots\cdots (10)$$

The output of the cell block, $\mathrm{I}^t_{\mathrm{N}i,j}$, which corresponds to the center coordinates of the target pattern, $p^t(i,j)$, can be obtained from the NMOSFET $M1$.

5. Simulation

Firstly, to confirm the algorithm of the proposed circuit, numerical simulations were performed concerning 16×16-pixel input images shown in Fig.9. In Fig.9 (b), a

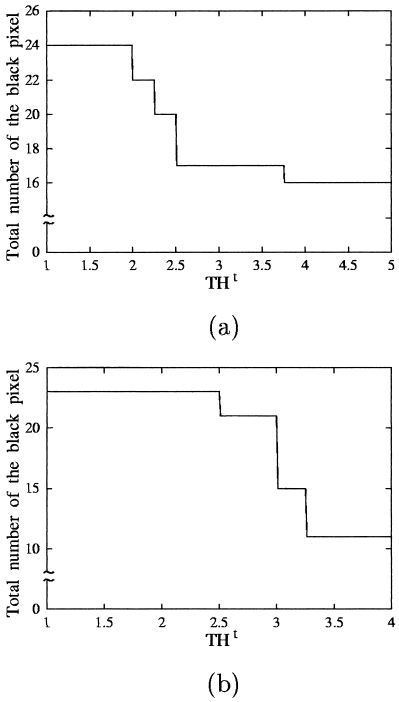

Fig.11 Number of the black pixels for the threshold value TH^t. (a) Image-1. (b) Image-2.

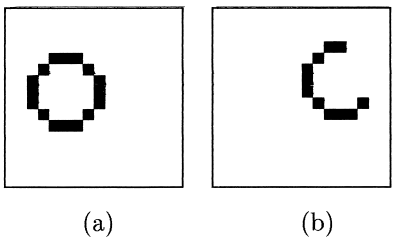

Fig.12 Noise elimination results for the input images shown in Fig.9. (a) Image-1. (b) Image-2.

part of the circular pattern is missing. Figure 10 shows the summation of the connection weights for $f^t(i,j)$. In Fig.10, the connection weights were set to $W_0 = 2$, $W_1 = 1$, $W_2 = 0.5$, and $W_3 = 0.25$. Figure 11 shows the total number of the black pixels for the threshold value TH^t. By setting the threshold value $TH^t \geq 4$, the proposed circuit can perform the noise elimination as shown in Fig.12. Figure 13 shows the summation of the connection weights for $g^t(i,j)$. Figure 14 shows the output image obtained by Fig.13. In Fig.14, the hatched pixels are those of the input image and the black pixel is the output of the proposed circuit. As one can see from Fig.14, the proposed circuit can extract the cell which corresponds to the center coordinates of the circular pattern.

In Figs.9 $\sim$ 14, the characteristics of the proposed algorithm were analyzed by numerical simulations. However, the non-ideal effects of the circuit implementation such as clock feedthrough, finite output resistance of the transistors, etc. cannot be analyzed by numerical simulations. Therefore, to analyze those non-ideal effects and to confirm the validity of the above-mentioned simplification, the SPICE simulations [14] were perfomed regarding to 8×8-pixel input images shown in Fig.15. In Fig.15, $1 \sim 64$ are labels to specify the coordinates of

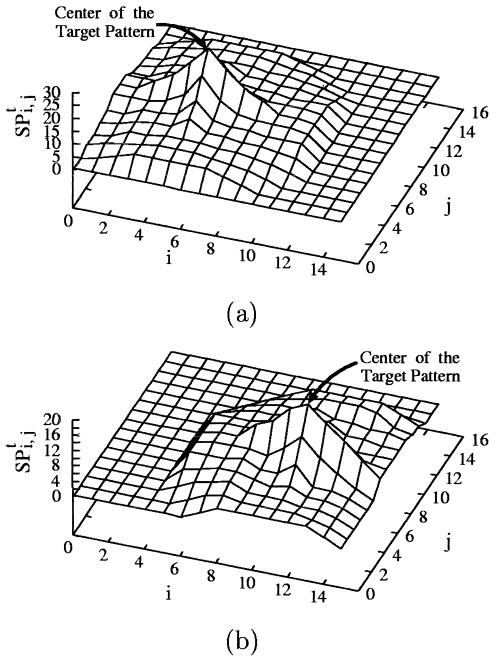

Fig.13 Summation of the connection weights for $g^t(i,j)$. (a) Image-1. (b) Image-2.

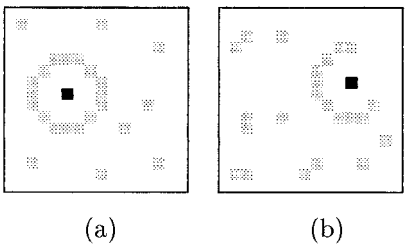

Fig.14 Output images obtained by the numerical simulations. (a) Image-1. (b) Image-2.

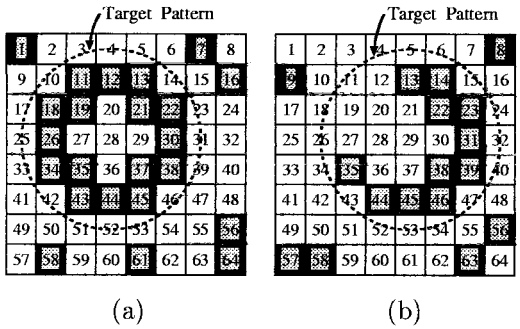

Fig.15 Input images used in SPICE simulations. (a) Image-1. (b) Image-2.

the cells. The SPICE simulations were performed under the conditions that the power supply was $V_{dd} = 5V$ and the bias current $Iu_{i,j}$ was 1 μA. In the proposed circuit shown in Fig.8, the ratios of the current mirrors were set to $W_0 = 1$, $W_1 = 0.5$, and $W_2 = 0.25$. Figures 16 and 17 show the transient characteristics for the proposed circuit. In SPICE simulations of Figs.16 and 17, the threshold currents were set to the values shown in Fig.18. From 0 μs to 5 μs, the proposed circuit functions as a noise elimination circuit. And from 5 μs to 10 μs, the proposed circuit functions as an extraction cir-

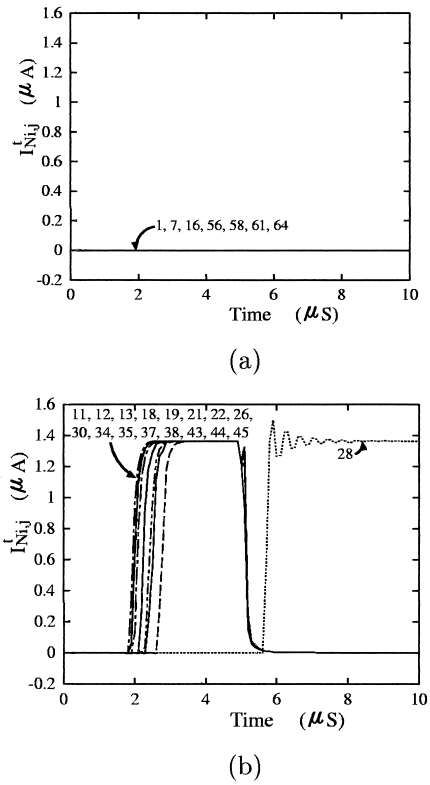

Fig.16 Transient characteristics of the proposed circuit for the input image-1. (a) Noise elimination result. (b) Extraction result.

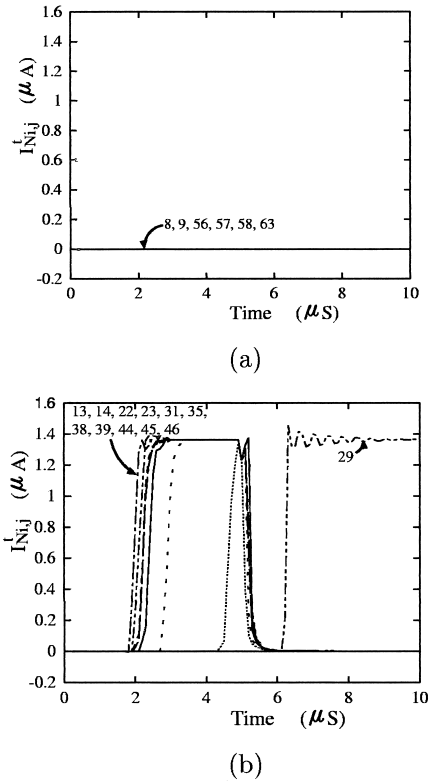

Fig.17 Transient characteristics of the proposed circuit for the input image-2. (a) Noise elimination result. (b) Extraction result.

cuit. Figures 16 (a) and 17 (a) show that the proposed circuit can eliminate the small clusters. Figures 16 (b) and 17 (b) show that the proposed circuit can extract the cell which corresponds to the center coordinates of the circular pattern. From Figs.16 and 17, the settling time of the proposed circuit was less than 10 μs. †

6. Discussion

In the past, several methods have been proposed for hardware implementation of a pattern recognition system. C.H.Chou et al. adopted an SIMD parallel algorithm to realize translation-invariant pattern recognition. Y.Tokunaga et al. proposed FPGA implementable pattern recognition system. The key idea of this method is a table look-up method for contraction of the stored pattern. The table look-up method enables the memory saving as well as exemption from the use of multipliers. On the other hand, the advantages of the proposed method are as follows: 1. The proposed circuit can be implemented on the hardware of an economical scale since the template patterns and the multipliers are not required. 2. By employing current mode techniques, extendability of the circuit and high-speed parallel processing can be achieved easily. Table 1 shows the comparison of the above mentioned methods.

7. Conclusion

A fuzzy based circuit to recognize circular patterns is proposed in this paper. The performance of the proposed circuit was confirmed by computer simulations. SPICE simulation results showed the following results:

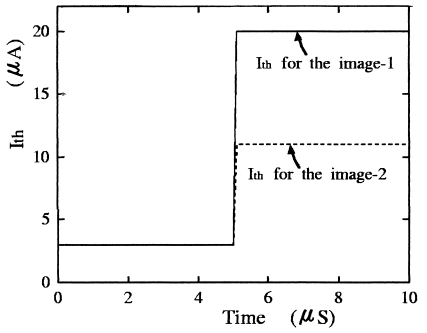

Fig.18 Threshold current I_{th}. (a) Image-1. (b) Image-2.

Table1 Comparison concerning the pattern recognition circuits.

	Proposed method	Chou et al.'s method	Tokunaga et al.'s method
Target of implementation	Analog circuit	Digital circuit	FPGA
High-speed processing	Yes	Yes	No*
Noise immunity	Yes	Yes	No
Exemption from template pattern	Yes	No	No
Circuit extendability	Yes	No	No
Invariance to transformation	Rotation	Translation	Translation & scaling

* The processing speed of this method which depends on the size of the input image is around $20ms$ for a 32×32-pixel image. The processing speed of other methods is independent from the size of the input image since the parallel operation can be available.

† These results depend on the device parameters of the MOSFETS, the values of the current sources, and so on. However, the processing speed is independent from the size of the input image since the circuit structure employing current-mode techniques enables the parallel operation.

1. The settling time of the proposed circuit was less than 10 μs. 2. Thanks to exemption from the use of template patterns as well as multipliers, the proposed circuit can be realized on the hardware of an economical scale. The proposed circuit is integrable by a standard CMOS technology and is similarly applicable to extract the center coordinates of a circular pattern from binary images.

An IC implementation of the proposed circuit is left to the future study.

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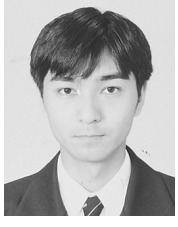

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