

Design of a discrete-time CNN using 1-dimensional chaos circuits with controllable nonlinear functions

Member	Kei EGUCHI	(Kumamoto National College of Technology)
Non-member	Yasukazu SEIKI	(Kumamoto National College of Technology)
Non-member	Toru TABATA	(Kumamoto National College of Technology)
Non-member	Hongbing ZHU	(Hiroshima Kokusai Gakuin University)
Member	Fumio UENO	(Kumamoto National College of Technology)
Member	Takahiro INOUE	(Kumamoto University)

In this paper, a discrete-time CNN using 1-dimensional chaos circuits with controllable nonlinear functions is proposed. The proposed CNN consists of $p \times q$ 1-dimensional chaos circuits which are called cell circuits. The nonlinear functions of the cell circuits can be controlled by employing fuzzy scheme. Thanks to the controllability of the nonlinear functions, the proposed circuit can adjust transition behavior of the CNN, electronically. Furthermore, the chaotic behavior of the cell circuit which is a portion of the proposed CNN is simple since the cell circuit is a 1-dimensional chaos circuit. To confirm the validity of the proposed CNN, two types of nonlinear dynamical phenomena are observed by SPICE simulations: chaos synchronization phenomenon and traveling wave phenomenon. The proposed CNN is integrable by a standard BiCMOS technology.

Keywords: chaos circuits, cellular neural networks, switched current, discrete-time circuits, analog circuits, integrated circuits

1. Introduction

Chaos is one of the most frequently encountered phenomena in the study of nonlinear dynamical systems. For this reason, to analyze and optimize the nonlinear dynamical systems, several approaches which exploit the chaotic behavior have been proposed. For example, Matsumura incorporated chaos into the movement of the mobile robot to avoid moving obstacles [1]. Alsing et al. attempted to control the chaotic behavior which exists in natural phenomena [2]. Among others, the studies employing CNNs (Cellular Neural Networks) which consist of chaos generators attract many researchers' attention. The CNN using chaos generators opens up new vistas for application systems, for example, models for the transport phenomena in biological and physical systems, shortest-path finding systems, and so on [3]-[8]. These studies exploiting CNNs have been realized on a digital computer. However, in case that the CNN consists of a large number of cells, the studies realized on a digital computer take a long computational time. For this reason, many researcher's have shown prototypes of the CNN using chaos circuits [4]-[7]. These CNNs exploit Chua's chaos circuits [9]-[11] as the cell circuits. Chua's circuit which is designed by voltage-mode techniques is one of the most famous 3-dimensional chaos circuits. Although the studies exploiting the CNNs can be achieved by employing Chua's circuit, the cell circuits which satisfy the following design aspects are desirable. 1. To control the transition behavior of the CNN, the flexibility of the cell circuit

such as controllability of the nonlinear function is desirable. 2. Simplicity of the chaotic behavior of the cell circuit is favorable since it enables the users to analyze the behavior of the network with ease. 3. To implement onto the chip, compatibility with a standard IC technology is desirable. These features enable the CNNs to get into experimental tools for the large scale networks.

In this paper, a discrete-time CNN using 1-dimensional chaos circuits with controllable nonlinear functions is proposed. The proposed CNN consists of $p \times q$ chaos circuits which are called cell circuits. The chaotic behavior of the cell circuit which is a portion of the proposed CNN is simple since the cell circuit is a 1-dimensional chaos circuit. The nonlinear functions of the cell circuits can be controlled by employing fuzzy scheme. Thanks to the controllability of the nonlinear functions, the proposed circuit can adjust transition behavior of the CNN, electronically. Furthermore, the cell circuit synthesized using switched-current (SI) techniques [12],[13] is suitable for integration since 1. SI circuits can be implemented by a standard digital process, 2. they exhibit low sensitivity to both temperature variations and supply voltage variations, and 3. they are more robust than voltage-mode counterparts against the reduction of the supply voltages. To confirm the validity of the proposed CNN, two types of nonlinear dynamical phenomena are observed by SPICE simulations: chaos synchronization phenomenon and traveling wave phenomenon.

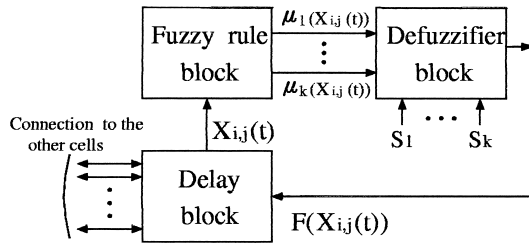


Fig.1 Block diagram of the cell circuit.

2. Architecture

The proposed CNN consists of $p \times q$ 1-dimensional chaos circuits called cell circuits. The dynamics of the proposed CNN is based on the following equation:

$$X_{i,j}(t + 1) = F(X_{i,j}(t)) + Q, \dots\dots\dots (1)$$

where t is the cycle of the CNN, Q is the effect from other cells, and $F(\cdot)$ is a piecewise-linear function determined by fuzzy scheme.

Figure 1 shows the block diagram of the cell circuit which is a portion of the proposed CNN. The cell circuit consists of a fuzzy rule block, a defuzzifier block, and a delay block. In the fuzzy rule block, the matching degrees ${}^{i,j}W_n$'s are determined by the following equation:

$${}^{i,j}W_n = \mu_n(X_{i,j}(t)) \quad (n = 1, 2, \dots, k), \dots (2)$$

where n ($= 1, \dots, k$) denotes the fuzzy label [14] for the input $X_{i,j}(t)$ and μ_n 's are the triangular membership functions [15].

In the defuzzifier block, the output fuzzy set, ${}^{i,j}W_1/{}^{i,j}S_1 + \dots + {}^{i,j}W_k/{}^{i,j}S_k$, is defuzzified by the center of area (COA) method [16], where ${}^{i,j}S_n$ is the singleton's element [16], $/$ is Zadeh's separator, and $+$ is the union operation. The defuzzified output $F(X_{i,j}(t))$ is given by

$$F(X_{i,j}(t)) = \frac{\sum_{n=1}^k {}^{i,j}S_n {}^{i,j}W_n}{\sum_{n=1}^k {}^{i,j}W_n}, \dots\dots\dots (3)$$

$$\triangleq \frac{\sum_{n=1}^k {}^{i,j}S_n {}^{i,j}W_n}{C}.$$

This defuzzified output $F(X_{i,j}(t))$ is obtained as the output of the defuzzifier block in Fig.1. To simplify the circuit, the membership functions are chosen such that the summation of the matching degree $\sum_{n=1}^k {}^{i,j}W_n$ in Eq.(3) becomes the constant value C . In the delay block, the output of the defuzzifier block is delayed by one cycle and it is fed back to the input of the fuzzy rule block. The connection to the other cells is realized in the delay block.

The functional blocks in Fig.1 will be implemented in the following section.

3. Circuit Structure

The proposed CNN is implemented by using switched-current (SI) techniques. The current-mode techniques are suitable for the implementation of CNN which consists of a large number of cells since they can realize the

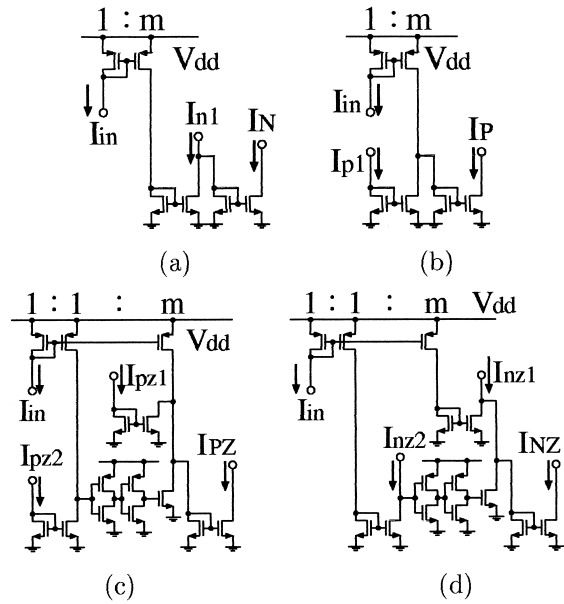


Fig.2 Membership function circuit (MFC). (a) N. (b) P. (c) PZ. (d)NZ.

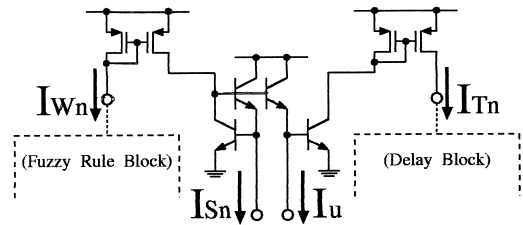


Fig.3 Translinear multiplier/divider circuit (TLC).

summation by wired-sum connection.

The fuzzy rule block in Fig.1 is realized by using membership function circuits (MFC's). Figure 2 shows CMOS membership function circuits. The synthesis of the membership function circuits is based on the following equations:

$$I_N = (I_{n1} - mI_{in}),$$

$$I_P = (mI_{in} - I_{p1}),$$

$$I_{PZ} = (mI_{in} \ominus I_{pz1})u(I_{pz2} - I_{in}),$$

$$I_{NZ} = (mI_{nz1} \ominus I_{in})u(I_{in} - I_{nz2}), \dots\dots\dots (4)$$

where $u(\cdot)$ is a unit step function, m is a parameter realized by the current-copying ratio of the current mirror, and \ominus is a bounded-difference operator defined as

$$\alpha \ominus \beta \triangleq \begin{cases} \alpha - \beta & \text{if } \alpha > \beta, \\ 0 & \text{if } \alpha \leq \beta. \end{cases} \dots (5)$$

Since $F(\cdot)$ in Eq.(1) is a piecewise-linear function, the triangular membership functions in Eq.(4) are chosen.

The defuzzifier block in Fig.1 is realized by using translinear multiplier/divider circuits (TLC's). Figure 3 shows the translinear multiplier/divider circuit. The TLC in Fig.3 realizes the following equation:

$$I_{Tn} = \frac{I_{Sn}}{I_u} I_{Wn}, \dots\dots\dots (6)$$

where $I_{Wn} \geq 0$, $I_{Sn} \geq 0$, and $I_u > 0$. Although multiplier/divider circuits can be constructed with

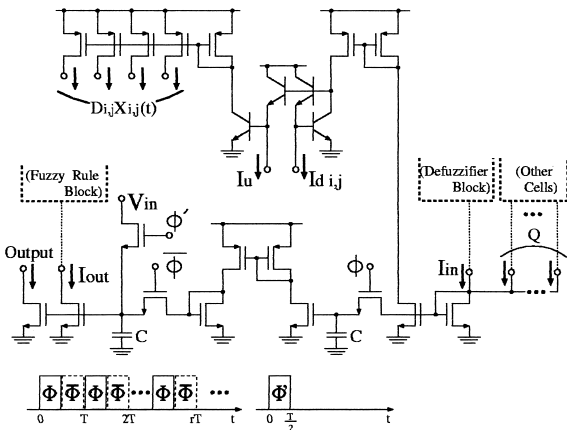


Fig.4 SI track & hold circuit (THC).

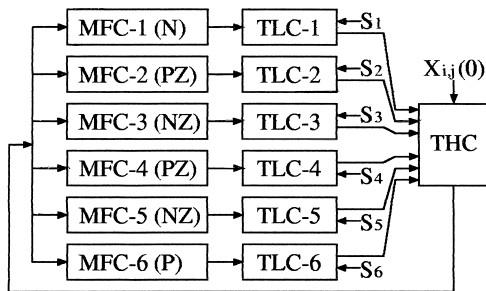


Fig.5 Block diagram of the cell circuit used in SPICE simulations.

MOSFET's instead of bipolar transistors, the multiplier/divider circuits constructed with bipolar transistors can realize high-linearity compared with those constructed with the MOSFET's. Moreover, the multiplier/divider circuit constructed with bipolar transistors has a very simple circuit structure and is suitable for lowering the supply voltages.

The delay block in Fig.1 is realized by an SI track & hold circuit (THC). Figure 4 shows the THC. The timing of a unit delay is controlled by the switches ϕ and $\bar{\phi}$. The THC realizes the wired-sum connection to the other cells as well as the unit delay. In the THC, the diffusion coefficient $D_{i,j}$ is realized by the following equation:

$$D_{i,j} = \frac{I_{d,i,j}}{I_u} \dots \dots \dots (7)$$

Hence, the connection to the other cells is close when the $I_{d,i,j} = 0$. In the delay block, the initial value $X_{i,j}(0)$ of the cell circuit is given by V_{in} .

4. Simulation

To confirm the validity of the circuit design, SPICE simulations [17] were performed regarding to the proposed circuit. As the examples of nonlinear dynamical phenomena, chaos synchronization phenomenon and traveling wave phenomenon were observed. In SPICE simulations, SI cell circuit shown in Fig.5 was used. The cell circuit used in SPICE simulations consists of 6 membership function circuits, 6 translinear multiplier/divider circuits, and an SI track & hold circuit. The cell circuit shown in Fig.5 can realize the nonlinear function which has 4 boundary points. SPICE

Table 1. Current values for the membership functions in Fig.2.

Building Block	Current Sources
MFC-1 (N)	$I_{n1} = 8.8\mu A$
MFC-2 (PZ)	$I_{pz1} = 2.9\mu A, I_{pz2} = 0\mu A$
MFC-3 (NZ)	$I_{nz1} = 3.2\mu A, I_{nz2} = 17.8\mu A$
MFC-4 (PZ)	$I_{pz1} = 5.9\mu A, I_{pz2} = 9.7\mu A$
MFC-5 (NZ)	$I_{nz1} = 6.3\mu A, I_{nz2} = 27.0\mu A$
MFC-6 (P)	$I_{p1} = 19.3\mu A$

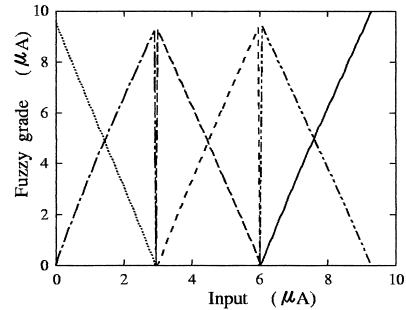
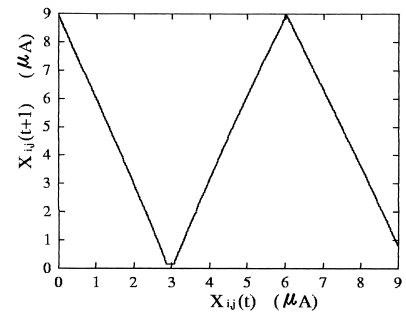
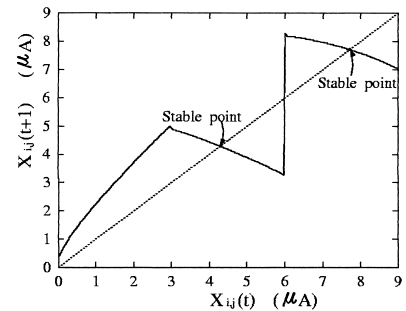


Fig.6 Membership functions used in SPICE simulations.



(a)

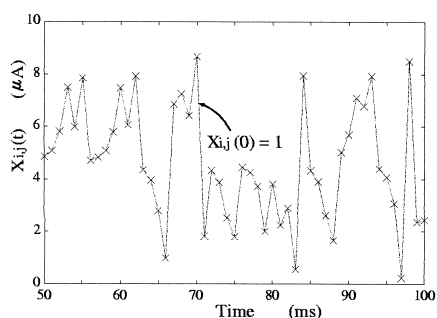


(b)

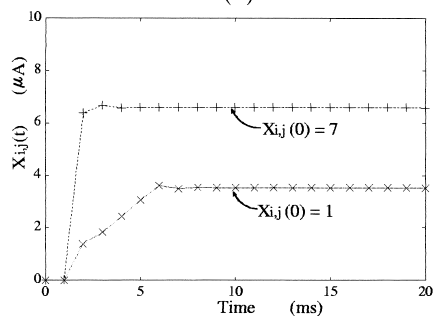
Fig.7 Nonlinear functions of the proposed cell circuit.

simulations were performed under the conditions that $V_{dd} = 5V$.

4.1 Cell Circuit Firstly, to confirm the validity of the circuit design, the SPICE simulations were performed concerning the SI cell circuit. Figure 6 shows the membership functions obtained by SPICE simulations. In this figure, the fuzzy-grade interval $[0, 1]$ is represented by $[0\mu A, 9\mu A]$. The ratio of the current mirror, m , in Fig.2 was set to $m = 3$. The current sources in the membership function circuits were set to the values shown in Table.1. Figure 7 shows the nonlinear functions of the SI cell circuit obtained by SPICE simulations. In Fig.7 (a), the current sources I_{S_n} 's (see in Fig.3) which correspond to the values of the singletons were set to $I_{S1}(=^{i,j} S_1) = 9\mu A, I_{S2}(=^{i,j} S_2) = 0\mu A, I_{S3}(=^{i,j} S_3) = 0\mu A, I_{S4}(=^{i,j} S_4) = 9\mu A, I_{S5}(=^{i,j} S_5) =$



(a)



(b)

Fig.8 Transient characteristics of the cell circuit.

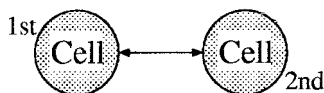
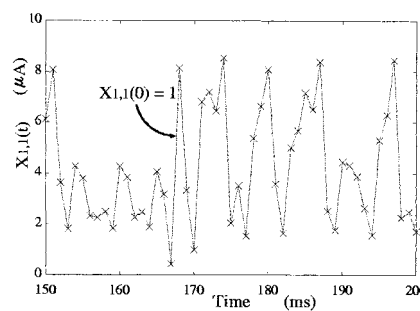


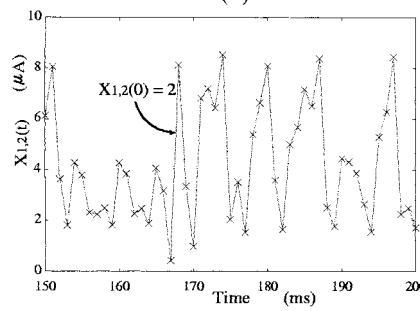
Fig.9 Architecture of the proposed CNN for chaos synchronization phenomenon.

$9\mu A$, and $I_{S6}(=^{i,j} S_6) = 0\mu A$. In Fig.7 (b), the current sources I_{S_n} 's were set to $I_{S1}(=^{i,j} S_1) = 0\mu A$, $I_{S2}(=^{i,j} S_2) = 3\mu A$, $I_{S3}(=^{i,j} S_3) = 3\mu A$, $I_{S4}(=^{i,j} S_4) = 1\mu A$, $I_{S5}(=^{i,j} S_5) = 7\mu A$, and $I_{S6}(=^{i,j} S_6) = 5\mu A$. The deformation of the nonlinear functions is due to the non-ideal effects of the SI circuits such as non-linearity of the transistors, offsets, etc.. However, the deformation of the nonlinear functions such as offset can be modified by controlling the values of the singletons. Figure 8 shows the output signals of the SI cell circuit obtained by SPICE simulations. In Fig.8, the output signals were generated by using the nonlinear function of Fig.7. As Figs.7 and 8 show, the behavior of the output signals of the SI cell circuit can be controlled electronically. In Fig.8 (a), the SI cell circuit generates the chaotic signal. The output signals in Fig.8 (b) converge to the values of the stable points. From Fig.8 (b), the nonlinear function of Fig.7 (b) has two stable points, P_r ($r = 1, 2$). The basin [6],[7] of the stable point, $B(P_r)$, is given by $B(P_1) = (0\mu A, 6\mu A)$ and $B(P_2) = [6\mu A, 9\mu A)$, where $P_1 = 3.5\mu A$ and $P_2 = 6.5\mu A$.

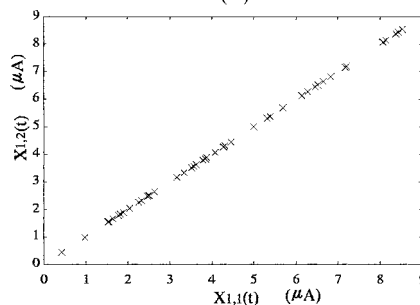
4.2 Chaos Synchronization Phenomenon To observe the chaos synchronization phenomenon, SPICE simulation was performed regarding to mutually-coupled cell circuits which consists of 2 cell circuits. Figure 9 shows the circuit architecture of the CNN to observe the chaos synchronization phenomenon. The dynamics of the proposed CNN in Fig.9 is given by



(a)



(b)



(c)

Fig.10 Chaos synchronization phenomenon obtained by SPICE simulation. (a) Output signal of the 1st cell circuit. (b) Output signal of the 2nd cell circuit. (c) Phase plot of the output signals of the proposed CNN.

$$\begin{aligned}
 X_{1,1}(t+1) &= \left(\sum_{n=1}^6 {}^{1,1}S_n {}^{1,1}W_n \right. \\
 &\quad \left. + \sum_{n=1}^6 {}^{1,2}S_n {}^{1,2}W_n \right) / 2C, \\
 X_{1,2}(t+1) &= \left(\sum_{n=1}^6 {}^{1,2}S_n {}^{1,2}W_n \right. \\
 &\quad \left. + \sum_{n=1}^6 {}^{1,1}S_n {}^{1,1}W_n \right) / 2C, \dots\dots (8)
 \end{aligned}$$

where C was set to $C = 9\mu A$. The SI cell circuits were connected via terminal Q (see in Fig.4). In the SPICE simulation for chaos synchronization phenomenon, the current sources I_{S_n} 's which correspond to the values of the singletons were set to the same values used in Fig.7 (a). Figure 10 shows the output signals of the mutually-coupled cell circuits. In the SPICE simulation of Fig.10, the initial values of the 1st and 2nd cells were set to $X_{1,1}(0) = 1\mu A$ and $X_{1,2}(0) = 2\mu A$, respectively. From Fig.10, the proposed CNN is useful as an experimental

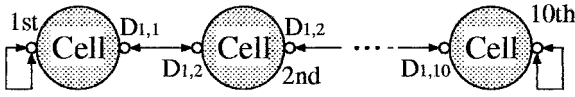


Fig.11 Architecture of the proposed CNN for traveling wave phenomenon.

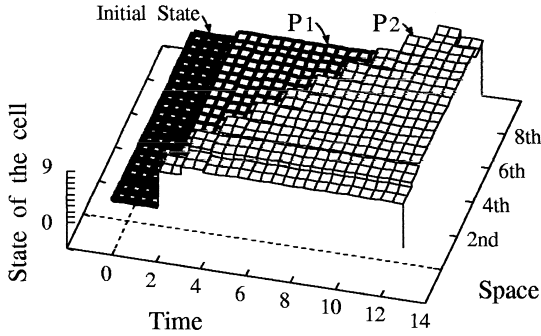


Fig.12 Simulated traveling wave in a chain of 10 cell circuits.

tool for chaos synchronization system.

4.3 Traveling Wave Phenomenon To observe the traveling wave phenomenon, SPICE simulation was performed regarding to a chain of 10 SI cell circuits. Figure 11 shows the circuit architecture of the CNN to observe the traveling wave phenomenon. The dynamics of the proposed CNN in Fig.11 is given by

$$\begin{aligned}
 X_{i,j}(t+1) = & \left(\sum_{n=1}^6 i,j S_n i,j W_n \right) / C \\
 & + D_{i-1,j} \left(\sum_{n=1}^6 i-1,j S_n i-1,j W_n \right) / C \\
 & + D_{i+1,j} \left(\sum_{n=1}^6 i+1,j S_n i+1,j W_n \right) / C,
 \end{aligned}$$

where C was set to $C = 9\mu A$. In the SPICE simulation for traveling wave phenomenon, the singletons of the SI cell circuits were set to $I_{S1}(=^{i,j} S_1) = 2\mu A$, $I_{S2}(=^{i,j} S_2) = 0\mu A$, $I_{S3}(=^{i,j} S_3) = 4\mu A$, $I_{S4}(=^{i,j} S_4) = 3\mu A$, $I_{S5}(=^{i,j} S_5) = 3\mu A$, and $I_{S6}(=^{i,j} S_6) = 2\mu A$. The SI cell used in this SPICE simulation has two stable points, P_r ($r = 1, 2$). The basin of these stable points, $B(P_r)$, is given by $B(P_1) = (0\mu A, 3\mu A)$ and $B(P_2) = [3\mu A, 9\mu A)$, where $P_1 = 1.2\mu A$ and $P_2 = 5.4\mu A$. Figure 12 shows the traveling wave in a chain of 10 SI cell circuits. In the SPICE simulation of Fig.12, the initial state of the 1st cell was set to P_2 and the initial states of all the other cells were set to P_1 . In Fig.12, the parameters $D_{i,j}$'s were set to $1/5$. Figure 13 shows the states of the SI cell circuits obtained by the SPICE simulations. From Figs.12 and 13, the traveling wave has propagated to the 10th cell after $12 ms$.

5. Discussion

In the past, several types of CNNs using chaos circuits have been proposed. Among others, V.Pérez-Muñuzuri et al. adopted Chua's chaos circuit to realize CNN using chaos circuit [5],[6]. By employing Chua's chaos circuit, this CNN can demonstrate binary-valued traveling wave phenomena. The cell circuit of this CNN is

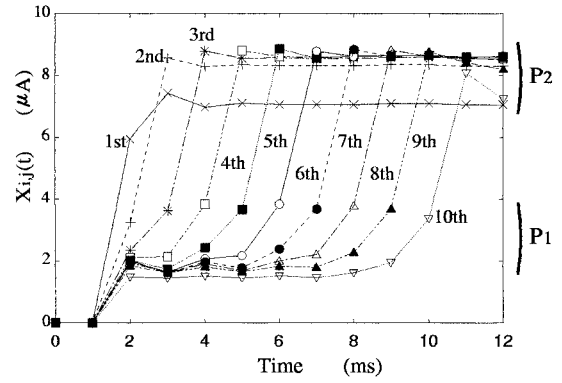


Fig.13 States of the cell circuits obtained by SPICE simulation.

Table2 Comparison.

	Proposed circuit	V.Pérez-Muñuzuri et al.'s circuit
Implementation technique	Current-mode	Voltage-mode
Type of output signals	Discrete-time	Continuous-time
Dimension of cell circuit	1-dimension	3-dimensions
Flexibility of cell circuit	Yes*	No

* The proposed CNN can control the nonlinear functions of cell circuits, electronically. Muñuzuri et al.'s model has to replace the components such as linear resistors, OTA's, etc. to control the behavior of the CNN.

a 3-dimensional continuous-time chaos circuit designed by voltage-mode techniques.

On the other hand, the advantages of the proposed method are as follows: 1. Thanks to the controllability of the nonlinear functions, the proposed circuit can adjust transition behavior of the CNN, electronically. 2. The chaotic behavior of the cell circuit which is a portion of the proposed CNN is simple since the cell circuit is a 1-dimensional chaos circuit. 3. The proposed cell circuit synthesized using switched-current (SI) techniques is suitable for integration since a) SI circuits can be implemented by a standard digital process, b) they exhibit low sensitivity to both temperature variations and supply voltage variations, and c) they are more robust than voltage-mode counterparts against the reduction of the supply voltages.

Table 2 shows the comparison of the above mentioned methods.

6. Conclusion

A discrete-time CNN using 1-dimensional chaos circuits with controllable nonlinear functions has been proposed in this paper.

The SPICE simulations concerning the proposed CNN showed the following results: 1. Thanks to the flexibility of the nonlinear functions, the dynamics of the proposed CNN can be controlled electronically. 2. The proposed CNN can demonstrate the chaos synchronization phenomenon as well as the traveling wave phenomenon.

The proposed CNN is integrable by a standard BiCMOS technology.

(Manuscript received February 25, 2000, revised

February 25, 2000)

References

- (1) K.Matsumura, "Simulation of obstacles avoidance by chaotic mobile robot using the deformed Bernoulli's map," *Trans. IEEJ*, vol.119-C, no.5, pp.603-614, May 1999.
- (2) P.M.Alsing, A.Gavrielides, and V.Kovanis, "Using neural networks for controlling chaos," *Physical Review E*, vol.49, no.2, pp.1225-1231, Feb. 1996.
- (3) R.R.Klevecz, J.Bolen, and O.Durán, "Self-organization in biological tissues: Analysis of asynchronous and synchronous periodicity, turbulence and synchronous chaos emergent in coupled chaotic array," *Int. J. Bifurc. and Chaos*, vol.2, no.4, pp.941-953, March 1992.
- (4) V.Pérez-Muñuzuri, V.Pérez-Villar, and L.O.Chua, "Traveling wave front and its failure in a one-dimensional array of Chua's circuits," *J. Circuits & Syst., and Comput.*, vol.3, no.3, pp.211-215, March 1993.
- (5) V.Pérez-Muñuzuri, V.Pérez-Villar, and L.O.Chua, "Autowaves for image processing on a two-dimensional CNN array of excitable nonlinear circuits: flat and wrinkled labyrinths," *IEEE Trans. Circuits & Syst.*, vol.40, no.3, pp.174-181, March 1993.
- (6) L.Pivka, "Autowaves and spatio-temporal chaos in CNNs—part I: a tutorial," *IEEE Trans. Circuits & Syst.*, vol.42, no.10, pp.638-649, Oct. 1995.
- (7) L.Pivka, "Autowaves and spatio-temporal chaos in CNNs—part II: a tutorial," *IEEE Trans. Circuits & Syst.*, vol.42, no.10, pp.650-664, Oct. 1995.
- (8) L.Nemes and T.Roska, "A CNN model of oscillation and chaos in ant colonies: a case study," *IEEE Trans. Circuits & Syst.*, vol.42, no.10, pp.741-745, Oct. 1995.
- (9) J.M.Cruz and L.O.Chua, "An IC chip of Chua's circuit," *IEEE Trans. Circuits & Syst.*, vol.40, no.10, pp.614-626, Oct. 1993.
- (10) K.Murali and M.Lakshmanan, "Effect of sinusoidal excitation on the Chua's circuit," *IEEE Trans. Circuits & Syst.*, vol.39, no.4, pp.264-270, April 1992.
- (11) J.M.Cruz and L.O.Chua, "A CMOS IC nonlinear resistor for Chua's circuit," *IEEE Trans. Circuits & Syst.*, vol.39, no.12, pp.985-995, Dec. 1992.
- (12) Takahiro Inoue, Kyoko Tsukano, Kei Eguchi, "Synthesis and Analysis of Chaotic Circuits Using Switched-Current Techniques," *IEICE Trans. on Fundamentals*, vol.E79-A, no.6, pp.758-763, Jun. 1996.
- (13) M.Degaldo-Restituto, F.Medeiro, and A.Rodríguez-Vázquez, "Nonlinear switched-current CMOS IC for random signal generation," *Electron. Lett.*, vol.29, no.25, pp.2190-2191, Dec. 1993.
- (14) L.A.Zadeh, "Fuzzy sets," *Information and Control*, vol.8, pp.338-353, 1965.
- (15) L.A.Zadeh, "Making computers think like people," *IEEE Spectrum*, pp.26-32, 1984.
- (16) L.A.Zadeh, "Outline of a new approach to the analysis of complex systems and decision process," *IEEE Trans. on Syst., Man, and Cybernetics*, vol.SMC-3, pp.28-44, 1973.
- (17) PSpice user's guide, MicroSim Corporation, 1989.

Kei Eguchi (Member) was born in Saga, Japan in 1972. He received the B.E., the M.E., and the D.E. degree from Kumamoto University, Kumamoto, Japan in 1994, 1996, and 1999, respectively. Presently he is a lecturer in Kumamoto National College of Technology. His research interests include nonlinear dynamical systems, intelligent circuits and systems, and low-voltage analog integrated circuits. He is a member of IEICE.



Yasukazu SEIKI (Non-member) received the B.S., M.S. degrees in Engineering from the University of Yamaguchi in 1966 and 1968, respectively. He worked for the University of Nagasaki from 1968 to 1988. Presently, he is an associate professor at the Department of Computer Sciences and Technology, Kumamoto National College of Technology. His research interests include agent-oriented circuit design, FPA design for intelligent circuits, and applications



of chaos circuits.

Toru Tabata (Non-member) was born in Kumamoto, Japan in 1946. He received the B.E., the M.E., and the D.E. degree in electrical engineering from Kumamoto University, Kumamoto, Japan, in 1970, 1972, and 1999, respectively. Currently, he is a Professor of the Department of Electronic Control at Kumamoto National College of Technology. His research interests and activities include the multiple-valued computer arithmetic circuits.



Hongbing ZHU (Non-member) received the B.S. and M.S. degrees in Electrical Engineering & Computer Science, from Wuhan Yejin University, Wuhan, P. R. of China, in 1982 and 1988, respectively. From 1982 to 1991 he was an Assistant and Lecturer of Wuhan Yejin University of Science and Technology. He worked as a visiting scholar at Kyushu Tokai University, Japan and Kumamoto University, Japan, in 1991 and 1992, respectively. He obtained a Ph.D. degree from Kumamoto University, in 1996. He is now a lecturer of Hiroshima Kokusai Gakuin University, Japan. His research interests include neural networks and high-speed processing, etc..



Fumio Ueno (Member) received the B.E. degree in electrical engineering from Kumamoto University, Kumamoto, Japan, in 1955, and M.E. degree and D.E. degree from Kyusyu University Fukuoka, Japan, in 1964, 1968 respectively. He was the faculty of Kumamoto University, where he was a Professor, Dean in 1992. Since 1994 he has been the President at Kumamoto National College of Technology, and IEICE Kyusyu Branch Chair in 1995. His main interest lies in the field of active networks.



Takahiro Inoue (Member) received the B.E. and the M.E. degree from Kumamoto University, Kumamoto, Japan in 1969 and 1971, respectively, and the D.E. degree from Kyushu University, Fukuoka, Japan in 1982. From 1971 to 1974, he worked as a Research Staff at Hitachi, Ltd., Yokohama, Japan. In 1975, he joined the faculty of Kumamoto University, where he is now a Professor. Dr. Inoue's current research interests include switched-capacitor/switched-current filters, continuous-time IC filters, low-power/low-voltage analog integrated circuits, and analog/digital intelligent circuits and systems. He is a member of the Institute of Electrical and Electronics Engineers and he served as an Associate Editor of *Transactions on Fuzzy Systems* during 1994-1996.

