Paper

Load Balancing Control by Symmetrical Coordinates Frame for PWM Inverter Based Reactive Power Compensators

Student member	Alper Akdağ	(Chiba Institute of Technology)
Member	Susumu Tadakuma	(Chiba Institute of Technology)
Member	Hideaki Minakata	(Chiba Institute of Technology)

This paper describes considerations on a Voltage Source Inverter based Reactive Power Compensator, especially load balancing control by symmetrical coordinates frame. Analytical expressions are derived to design the current controllers. With the designed controllers, fast response to the step changes in the reference current values can be obtained. This results in the improvement of the overall system performance. The improved current tracking capabilities of the inner controllers and better performance characteristics of dc voltage and reactive power loops are demonstrated for steady state and transient conditions. Besides this, the required additional loops for load balancing property of the VSI based SVC are investigated by using the positive - negative sequence decomposition calculated in α-β reference frame which gives a faster response than the separation in d-q frame. Simulation results have shown that with the use of simple additional loops, VSI type SVC can also achieve load balancing besides VAR compensation and dc voltage regulation.

Keywords: Flexible AC Transmission System (FACTS), reactive power compensation, static shunt compensator, unbalanced load, negative and positive sequence components

1. Introduction

Variable reactive power compensation is an important issue for transmission and distribution systems. First developed Static VAR Compensators (SVC) were designed as Thyristor Switched Capacitors (TSC) or Thyristor Controlled Reactors (TCR) [1]. Recently, the use of switching power converters as reactive power compensators is gaining popularity. The absence of large energy storage elements is the main advantage of these compensators. They have the features of

i. avoiding the risk for potential resonance conditions,
ii. increasing the response speed,
iii. reducing the total system real estate [2,3].

One of the power electronics devices used for compensation purposes, is the Voltage Source Inverter (VSI) [2]-[10]. VSI is connected to the power system through three phase inductors (or three phase transformers) as shown in Fig. 1. The reactive power supplied or absorbed by the VSI based compensator is controlled by adjusting the inverter output voltage magnitude to less than or greater values than the system voltage. The dc voltage across the dc link capacitor is controlled by the phase angle of the generated voltage with respect to system voltage.

In the literature, VSI based SVC's and their control systems are investigated in different aspects. [4], [5] and [6] give a detailed modeling of controllers based on the linearization process of the non-linear equations. In [2], a neural network control principle is applied for VSI based SVC. A multilevel VSI is applied to SVC operation to obtain better operating performance in [3]. The operating and control principles in these compensators are complicated and difficult to implement. In this paper, a simple mathematical model of the VSI based compensator will be presented. With the use of this model, a controller with decoupling principle will be designed and the optimum control parameters will be investigated. Theoretical settling times and overshoot of current controllers have been calculated and compared with the results obtained by simulations and experiments. As a final step, the necessary additional loops for the controller will be designed to use the compensator also for load balancing purposes. The control system has been designed in d-q frame, but the decomposition of positive and negative sequence components have been done in α-β reference frame. By that way, a more reliable and stable control has been obtained. Besides the theoretical studies, this paper is also furnished with the simulation and experimental results.

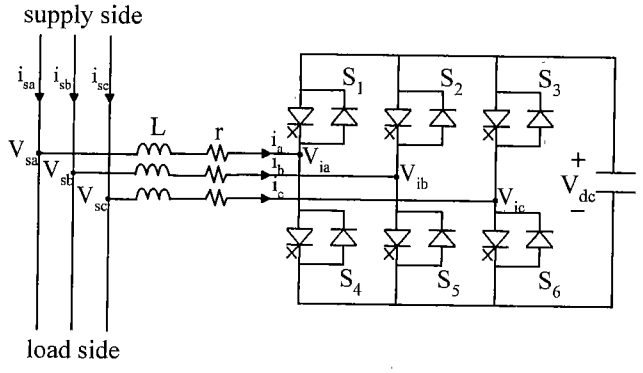

Fig. 1. VSI Based Reactive Power Compensator

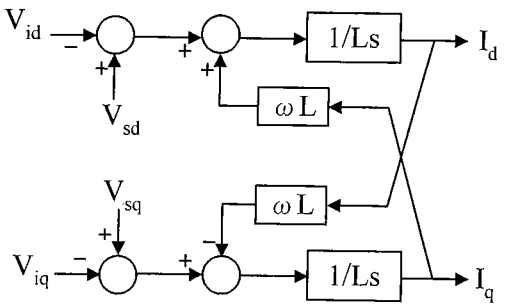

Fig. 2. Block diagram representation of the physical system

2. Mathematical Model of the Compensator

In order to obtain a controller for the compensator shown in Fig.1, first a mathematical model is derived. During the analysis and the design of the controller, rotating axis transformation parameters (i.e. d-q-0) are used. This axis transformation is chosen instead of stationary axis transformation because in this method, sinusoidal voltages and currents are transformed into dc quantities in the steady state conditions. By this way, it is easier to obtain the optimum values for the controller parameters (e.g. K and τ for a PI controller).

From Fig.1, the voltage equations can be written in stationary a-b-c frame as;

$$\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = \begin{bmatrix} L\dfrac{di_a}{dt} \\ L\dfrac{di_b}{dt} \\ L\dfrac{di_c}{dt} \end{bmatrix} + \begin{bmatrix} V_{ia} \\ V_{ib} \\ V_{ic} \end{bmatrix} \quad \text{.....(1)}$$

where i_a, i_b, i_c are the compensating currents, and V_{ia}, V_{ib}, V_{ic} are the generated voltages by the inverter. The equations in (1) can be written by assuming that i) the power system is a balanced 3-phase system, ii) there is no harmonics flowing in the system, and iii) the value of the resistance value is small and therefore negligible.

The equations in (1) are transformed into the stationary α - β frame as in (2) by the use of transformation matrix in (3).

$$\begin{bmatrix} V_{s\alpha} \\ V_{s\beta} \end{bmatrix} = \begin{bmatrix} L\dfrac{di_\alpha}{dt} \\ L\dfrac{di_\beta}{dt} \end{bmatrix} + \begin{bmatrix} V_{i\alpha} \\ V_{i\beta} \end{bmatrix} \quad \text{.....(2)}$$

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad \text{.....(3)}$$

Transformation from α - β frame to rotating d-q frame can be obtained as follows;

$$\begin{bmatrix} d \\ q \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix}\begin{bmatrix} \alpha \\ \beta \end{bmatrix} \quad \text{.....(4)}$$

Applying (4) into (2) (see Appendix A for details), the voltage equations in the rotating axis frame can be obtained as:

$$\begin{bmatrix} V_{sd} \\ V_{sq} \end{bmatrix} = \begin{bmatrix} L\dfrac{di_d}{dt} \\ L\dfrac{di_q}{dt} \end{bmatrix} + \omega L\begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} V_{id} \\ V_{iq} \end{bmatrix} \quad \text{....(5)}$$

Expanding (5) into its components, the following two differential equations can be obtained.

$$\begin{aligned} L\frac{di_d}{dt} &= V_{sd} - V_{id} + \omega L i_q \\ L\frac{di_q}{dt} &= V_{sq} - V_{iq} - \omega L i_d \end{aligned} \quad \text{.....(6)}$$

The equations in (6) are the model of the physical system which consists of a converter connected to an ac supply. In Fig. 2, block diagram representation of the physical system is shown.

3. Control System of the Compensator

As can be seen clearly from Fig. 2, current components are coupled through the term ω, and it is known that the reference current tracking capability of the controllers (such as PI controller) is not good and rapid enough for the coupled systems. In order to improve the performance and reduce the interaction between the active and reactive current controls, a decoupling controller is necessary. Inspection of (6) leads directly to a controller as in (7) that will provide decoupled control of i_d and i_q.

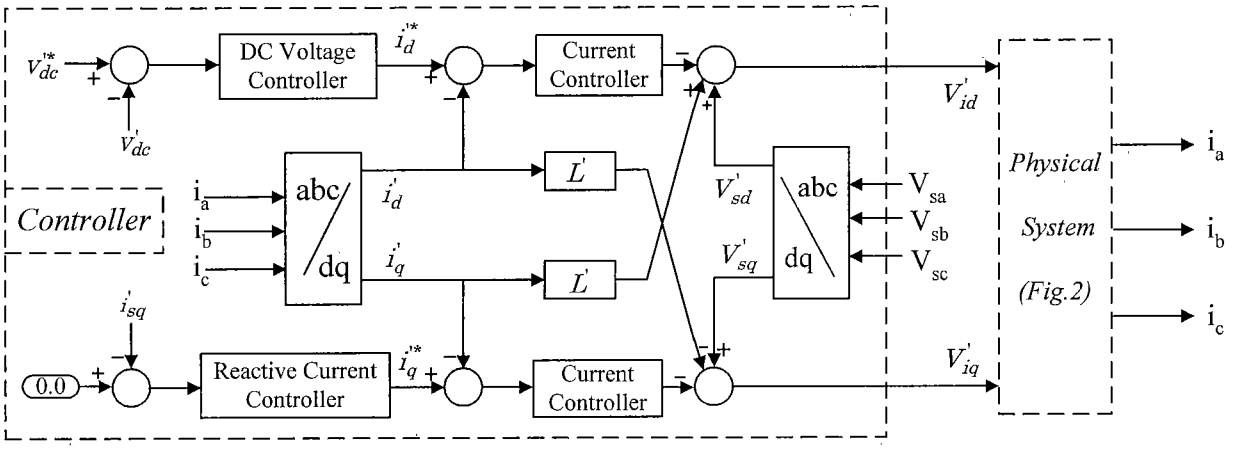

Fig. 3. Control block diagram of the VSI based compensator

$$\begin{aligned} V_{id} &= V_{sd} + \omega L i_q - \Delta d \\ V_{iq} &= V_{sq} - \omega L i_d - \Delta q \end{aligned} \quad \text{.....(7)}$$

where, Δ d and Δ q are the outputs of current controllers.

$$\begin{aligned} \Delta d &= (PI)(i_d^* - i_d) = k_{id}\frac{1+\tau_{id}s}{\tau_{id}s}(i_d^* - i_d) \\ \Delta q &= (PI)(i_q^* - i_q) = k_{iq}\frac{1+\tau_{iq}s}{\tau_{iq}s}(i_q^* - i_q) \end{aligned} \quad \text{.....(8)}$$

where (PI) corresponds to Proportional-Integral control principle. These two signals are generated by the effects of outer loops for V_{dc} and supply reactive current, and they generate additional voltages in transient states.

Inserting (7) to (6), (9) can be obtained which represents the input-output relation of the VSI based compensator system.

$$\begin{aligned} L\frac{di_d}{dt} &= \Delta d \\ L\frac{di_q}{dt} &= \Delta q \end{aligned} \quad \text{.....(9)}$$

From the above equations, it can be seen that both d and q components of the compensating currents can be controlled independently, and by the use of PI controllers it is possible to obtain good dynamics and steady state performance. By applying a PI controller with a transfer function of $(k_{id}\frac{1+\tau_{id}s}{\tau_{id}s})$, the closed loop transfer function can be obtained as follows.

$$\frac{\Delta i_d}{\Delta i_d^*} = k_{id}\frac{s\tau_{id}+1}{s^2\tau_{id}L + sk_{id}\tau_{id} + k_{id}} \quad \text{.....(10)}$$

Since the transfer function in (10) is a second order system transfer function, the damping ratio (ξ) and oscillation frequency (ω_n) can be written as:

$$\xi = \frac{1}{2}\sqrt{\frac{k_{id}\tau_{id}}{L}} \quad \text{.....(11)}$$

$$\omega_n = \sqrt{\frac{k_{id}}{\tau_{id}L}} \quad \text{.....(12)}$$

With the use of (11) and (12), it is straightforward to find the parameters of the PI controllers (k and τ) when the settling time (T_s) and maximum allowable overshoot values are specified.

Generally, settling time should be chosen as small as possible to provide fast response, but the limitation by the carrier frequency must be taken into account. The damping ratio should be within the limits of 0.6 and 1.0 i) to ensure 10% overshoot, and ii) not to limit the fast response. The same procedure is also applicable to the q-axis compensating current control system.

With these principles, the whole control block diagram of the compensator is given in Fig. 3, including the dc voltage and reactive power control loops. In the control system, a per-unit system has been adopted according to the following definitions.

$$i_x' = \frac{i_x}{i_{base}}, \quad V_{sx}' = \frac{V_{sx}}{V_{base}}, \quad V_{ix}' = \frac{V_{ix}}{V_{base}}$$

$$L' = \frac{\omega L}{Z_{base}}, \quad Z_{base} = \frac{V_{base}}{i_{base}}$$

4. Performance of the Control System

4.1 Simulation and Experimental Setup In order to verify the theoretical studies of Section 3, and observe the capability of the control system, simulation and experimental studies have been carried out. For simulation purposes, an EMTDC electromagnetic transients simulation program is used. For the experimental studies, the system has been modeled by the use of a PC based Hybrid Simulator, as shown in Fig. 4. With this experimental setup, a C program for the proposed control system is written and compiled in the PC environment. Then the information is loaded to the "Interface & Calculation Unit" through the parallel port. The PWM gate signals are generated according to the magnitude and phase angle information from the control system.

The parameters of the power and the control system used in both simulation and experimental works are presented in Table I. The current controllers are designed to obtain zero steady-state error and an overshoot within the acceptable limits. On the other hand, the reactive current and dc voltage control loops' parameters are selected to obtain zero steady-state error and relatively larger settling time than the inner current loops.

4.2 Simulation and Experimental Results As simulation studies, the current tracking capabilities of the inner current loops are investigated besides the performance investigation of the reactive power and dc voltage loops. For this purpose, the following two cases are examined.

i) a step change in the supply current q-axis reference value (i.e. a change in the supply side reactive power value),

ii) an instantaneous increase in dc voltage reference.

Normal operation of an SVC requires zero reactive power in the supply side. However, for the examination of the transient characteristics of the control loops, reference value of the reactive current flowing in the supply side is changed from 0-pu (per unit) to 0.15-pu. The results obtained are demonstrated in Fig. 5. The q-axis current flowing to the inverter reaches its steady-state value within the settling time of about 2.5ms, which is dictated by the natural frequency (ω_n) and damping ratio (ξ) of the inner loop calculated according to (11) and (12). Since the reactive power loop is an outer loop of the control system, its settling time is chosen longer than the inner loop as seen from the same figure. It can be seen easily that the reactive power control and q-axis current control loops have good dynamic response against step changes in reactive current reference value.

In a VSI based compensator operation, there is generally no need for changing the dc voltage level across the capacitor, but for observing the d-axis current response characteristics, the reference value of the dc voltage level is increased instantaneously, to change the d-axis current reference value as shown in Fig. 6. A step increase of V_{dc} from 200V to 220V causes an instantaneous change in i_d^*. The inner current control loop causes i_d to track the reference current, i_d^*, by properly designed PI parameter values. In this study, settling time is adjusted to about 2msec. as can be seen from Fig. 6 that fits with the theoretical result obtained by the parameter values of Table 1.

To validate the simulation results of the proposed control system, experimental studies are carried out. The results are demonstrated in Figs. 7 and 8 for the similar changes in the power and control system parameters as in simulation studies. The results obtained by the experimental studies are in good accordance with the simulations. But, there are some slight differences that may be caused by the harmonic distortion of controlled currents (i.e. the influence of the converter), A/D conversion process and the discrete controllers affects. These reasons and possible uncertainties in the system parameters reduce slightly the system performance. Since it is beyond of this paper to discuss the improvement techniques such as current prediction algorithms, it is left as future work.

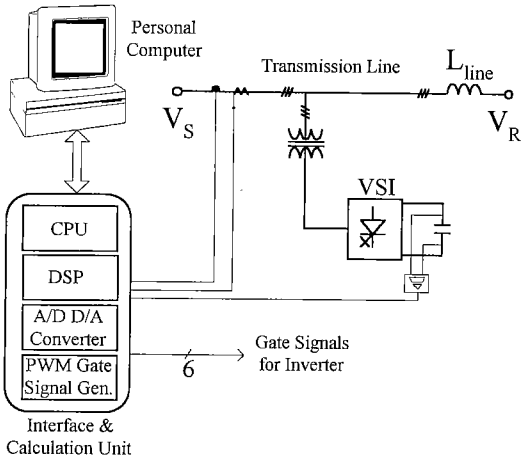

Fig. 4. Experimental setup

TABLE I POWER AND CONTROL SYSTEM PARAMETERS FOR SIMULATION AND EXPERIMENTAL STUDIES

Power Circuit	
Eqv. Inductance of Trans.	8mH
Inverter	4.2kVA
Capacitance	940uF
Supply Voltage	100Vrms (l-l)
3-phase Load	260Var, 0.76pf

Control Circuit	
id	K = 3.75 τ = 0.015
iq	K = 3.1 τ = 0.02
Vdc	K = 2.5 τ = 0.006
is_q	K = 2.0 τ = 0.006

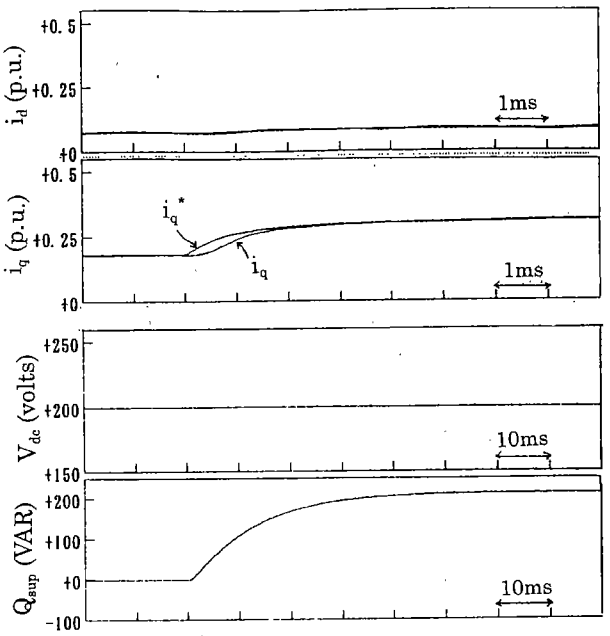

Fig.5. Simulation result for a step change in the supply side reactive current reference

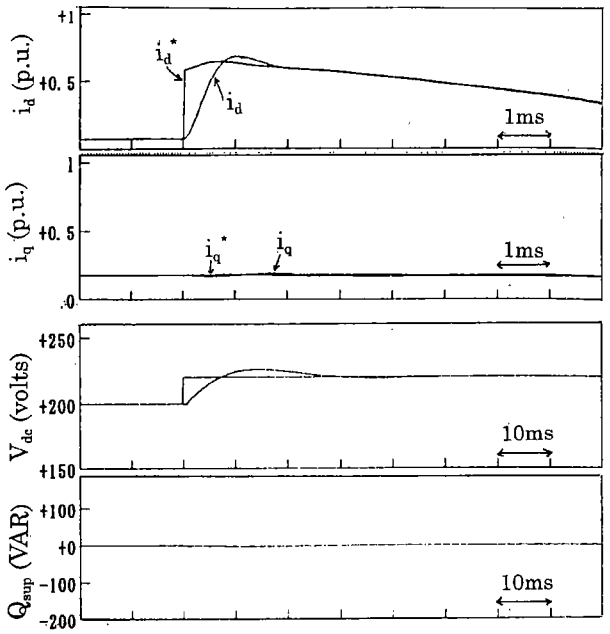

Fig. 6. Simulation result for a step change in the dc link voltage reference (200V → 220V)

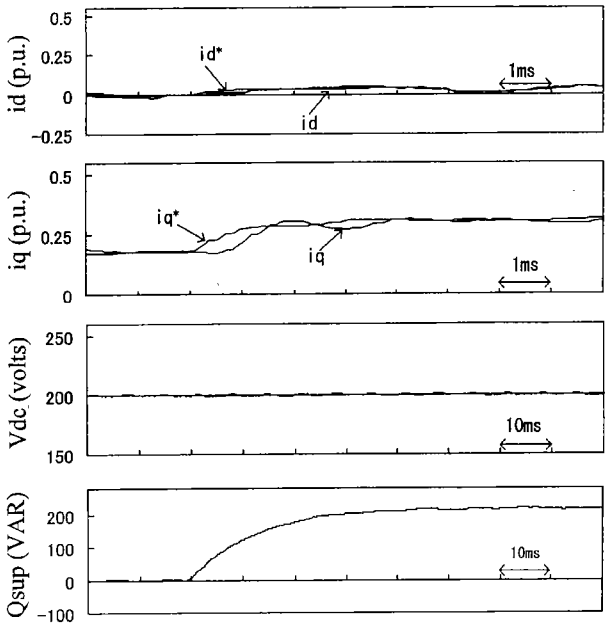

Fig.7. Experimental result for a step change in the supply side reactive current reference

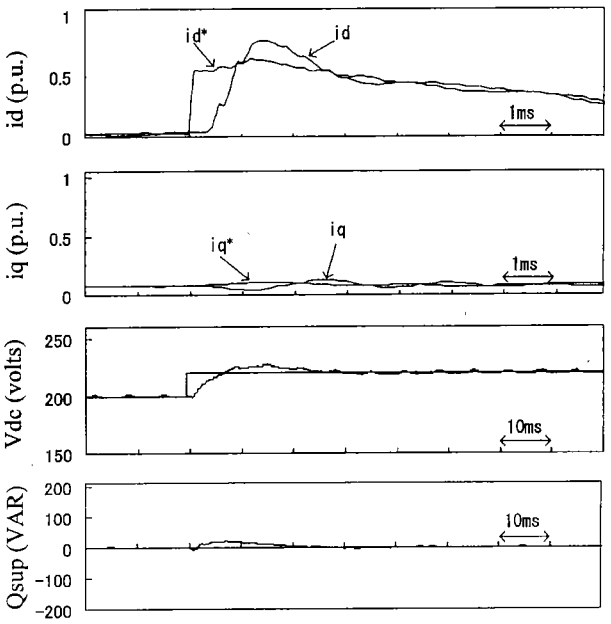

Fig.8. Experimental result for a step change in the dc link voltage reference (200V → 220V)

5. Load Balancing Principle of the Compensator

5.1 Unbalance Operation and its Effects

Most of ac power systems are three-phase and designed for balanced operation. In high quality power supply systems, "balanced phase currents and voltages" property must be held. In an unbalanced operation, negative and zero sequence components will also arise in addition to the positive sequence component.

These undesirable negative and zero sequence components cause additional losses in motors and generators, oscillating torques in ac machines, increased ripple in rectifiers, saturation of transformers, excessive neutral currents, malfunctioning of several types of equipments, etc. In order to minimize these undesirable effects caused by the unbalanced operating conditions to the other loads connected to the same point of common coupling, load balancing techniques must be applied.

In the following sections, the necessary additional control loops for the controller of an SVC in an unbalanced load condition will be investigated and the performance results will be given.

5.2 Decomposition to the Positive and Negative Sequence Components Decomposition of the electrical variables, such as currents and voltages, into the negative and positive sequence components can be done in different ways [11]-[13]. In most of the papers which are dealing with unbalanced loads (or unbalanced supply voltages) decompose the positive and negative sequence components in synchronously rotating frame (i.e. d-q frame). In this method, positive sequence d-q and negative sequence d-q components has dc components and additional ac signals oscillating with a frequency of the two times of the fundamental. These ac signals should be filtered with four low-pass or band-pass filters to obtain the real values for d-q components in positive and negative sequences. As it is obvious, addition of the filter circuits to the system imposes a delay to the controller which reduces the performance and may cause instability problems in most cases

In this paper, negative and positive sequence decomposition has been done in α-β frame without any need for filters that makes the controller faster and avoids the possible instability problems. In Appendix B, the basic principles of the two approaches are shown schematically.

An unbalanced system can be decomposed into two balanced three-phase systems as shown in Fig. 9. The positive and negative sequence load currents of this system can be modeled mathematically as in (13) and (14).

$$\begin{bmatrix} I_{+a} \\ I_{+b} \\ I_{+c} \end{bmatrix} = \begin{bmatrix} 1 \\ a^2 \\ a \end{bmatrix} I_+ \quad \text{.....(13)}$$

$$\begin{bmatrix} I_{-a} \\ I_{-b} \\ I_{-c} \end{bmatrix} = \begin{bmatrix} 1 \\ a \\ a^2 \end{bmatrix} I_- \quad \text{.....(14)}$$

where,

$$I_+ = \frac{1}{3}(I_a + aI_b + a^2 I_c),\ I_- = \frac{1}{3}(I_a + a^2 I_b + aI_c),$$

$$a = e^{j120} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}, \qquad a^2 = e^{j240} = -\frac{1}{2} - j\frac{\sqrt{3}}{2}.$$

By the use of (3), negative and positive sequence stationary α-β frame components can be obtained as in (15) and (16) respectively.

$$\begin{bmatrix} I_{-\alpha} \\ I_{-\beta} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} I_\alpha - jI_\beta \\ I_\beta + jI_\alpha \end{bmatrix} \quad \text{.....(15)}$$

$$\begin{bmatrix} I_{+\alpha} \\ I_{+\beta} \end{bmatrix} = \begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} - \begin{bmatrix} I_{-\alpha} \\ I_{-\beta} \end{bmatrix} \quad \text{.....(16)}$$

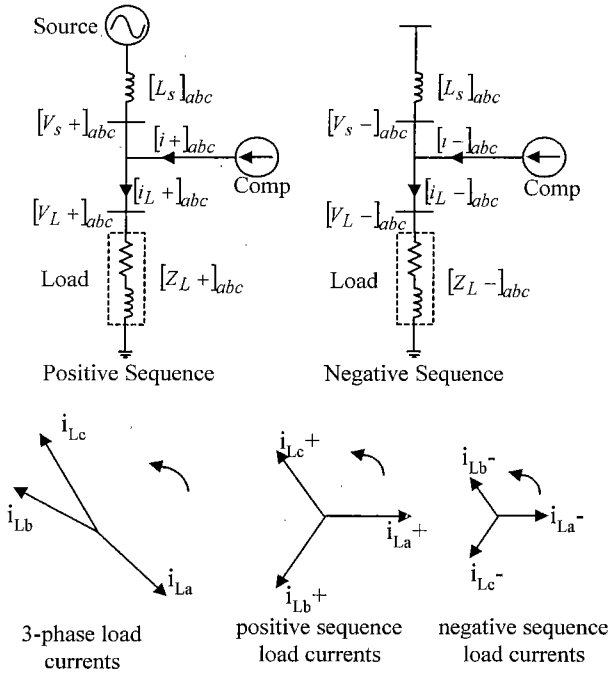

Fig.9. Positive and negative sequence equivalent circuit representation of the power system and the corresponding phasor diagrams

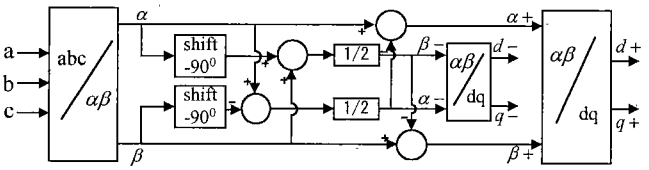

Fig.10. Decomposition to the positive and negative sequence components in α - β frame

d-q frame components for the positive sequences can be obtained by using the transformation matrix in (4) and for the negative sequence in (17). The negative and positive decomposition is demonstrated in blocks in Fig. 10.

$$\begin{bmatrix} d_- \\ q_- \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} \alpha_- \\ \beta_- \end{bmatrix} \quad \text{.....(17)}$$

5.3 Control System The control block diagram in Fig. 3 can be modified to allow compensation of the negative sequence components besides the normal operation of the VSI based compensator. The principle in the design of the new controller is adding the loops, which eliminates the negative sequence d-q components in the supply side currents. The additional d-q axis negative sequence controllers cause the generation of unbalanced voltages at the terminals of the inverter, which results in unbalanced compensating currents flowing to or from the compensator. The positive sequence components of these compensating currents do the

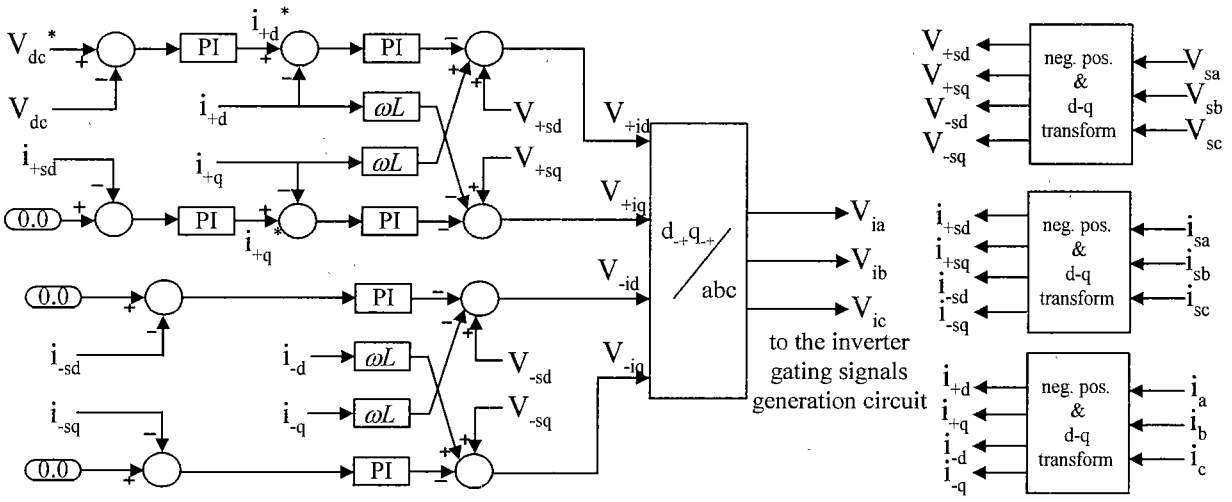

Fig.11. Control block diagram including load balancing control loops

usual job of the VSI based compensator, while the negative sequence currents are generated according to the unbalance factor of the load. The outputs of the control block which are used for the generation of gate signals of the inverter switches are transformed into stationary α-β coordinates as in (18), and then to stationary a-b-c coordinates. The whole control block diagram including the unbalanced load compensation principle is demonstrated in Fig. 11.

$$\begin{bmatrix} V_{i\alpha} \\ V_{i\beta} \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) & \cos(\omega t) & \sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) & -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} V_{+id} \\ V_{+iq} \\ V_{-id} \\ V_{-iq} \end{bmatrix} \quad \text{.....(18)}$$

5.4 Simulation Results In order to verify the load balancing capability of the VSI based compensator, simulation studies have been carried out. During these studies, balancing performance in an unbalanced load condition and the response in fault conditions of the compensator are investigated. To avoid any damage to the inverter of the experimental setup during a fault condition, only simulation studies are performed instead of experimental studies.

The load used in the first simulation circuit is composed of two parts. The first part of the load has a total reactive power of 200Var (lagging) and power factor of 0.87. At the time of 0.05sec., an unbalanced RL load with inductance values of 50mH and resistance values of 20, 10, and 5Ω are connected to the circuit with a circuit breaker. As can be seen from Fig. 12, before and after the connection of the unbalanced load to the system, SVC is compensating the reactive power of the load as well as regulating the dc voltage across the dc link capacitor. After t=0.05sec, besides these two duties, SVC also eliminates the negative sequence components of load currents which results in balanced supply line currents.

As a second simulation study, a line-to-ground fault is applied to the load side of phase-C. Results obtained are demonstrated in Fig. 13. The highly unbalanced load currents are balanced with the proper operation of the SVC. If the fault current flowing in the load side exceeds the limitations of the compensator, the load balancing capability can not be achieved properly. For comparison purposes, the performance of SVC without load balancing loops is illustrated for the same load and fault conditions in Fig. 14. As can be seen easily, besides the high harmonic content in the supply line currents, relatively high and unbalanced currents are flowing in the supply side.

The main disadvantage of the proposed control principle is the generation of unbalanced voltages at the inputs of the inverter. This results in unbalanced compensator line currents flowing through the coupling transformer. These 3-phase unbalanced line currents cause an ac ripple in the dc-link voltage with a frequency of the two times of the fundamental frequency. The amplitude of the oscillation becomes larger, if the load unbalance factor is higher. This phenomenon can be seen in Figs. 12 and 13. Since the load in Fig. 13 is highly unbalanced when compared to the load in Fig. 12, the ripple amplitude on the dc voltage is higher obviously. This ripple on the dc-link capacitor has the risk of causing resonance, if the power system and inverter parameters are not designed properly. To avoid such a resonance, the frequency of tank circuit, composed of the dc-link capacitor and the inductance of the transformer, should not coincide with the frequency of the ripple in the dc-link voltage. As an another solution for avoiding the risk of resonance, a tuned filter should be connected across the dc link capacitor, but such a solution increases the cost of the compensator. For that reason, this may not be a feasible solution for this kind of applications.

From the simulation studies, it can be concluded that the reactive power compensation and load balancing can be done by simple additions to the controller of the VSI based compensator. Its

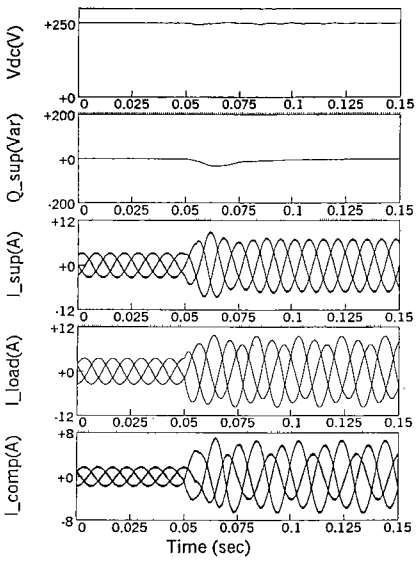

Fig.12. Simulation results for load balancing performance of SVC

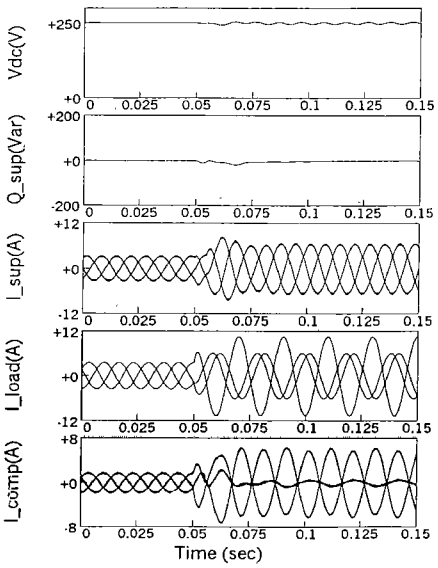

Fig.13. Response of the SVC for a single phase to ground fault (with load balancing control loops)

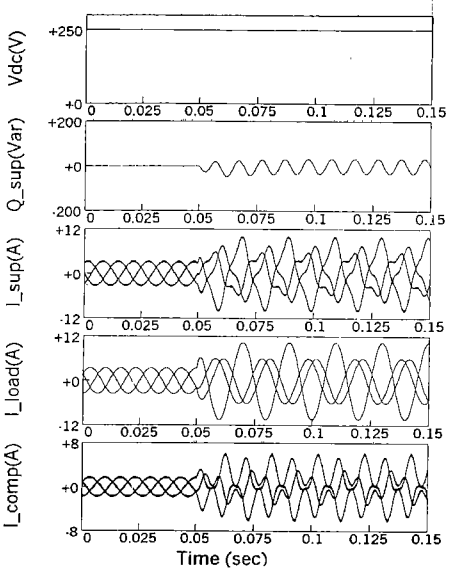

Fig.14. Response of the SVC for a single phase to ground fault (without load balancing loops)

performance is quite successful as seen from Figs. 12 and 13. Supply line currents are balanced within one cycle of supply voltage (20ms) for a step change from balanced to the unbalanced load current condition.

6. Conclusion

In this paper, a VSI based Reactive Power Compensator is presented for different load conditions with experimental and simulation results. It is shown that by a simple mathematical model, it is possible to determine the dynamics of the current control system (i.e. overshoot and settling time). Besides the reactive compensation of the SVC, it is shown that VSI based compensator is also an efficient tool for balancing the load and for avoiding the over-currents during fault conditions.

In the load balancing control circuit, the positive and negative sequence components decomposition is calculated in α-β frame instead of d-q frame, which is different from most of the control principles used extensively in the SVC. Using α - β frame in decomposition eliminates the need for low-pass filters as in the decomposition in d-q frame. This improves the performance of the controller and avoids possible instability problems. It is verified that decomposition in the α-β frame results in a good performance.

Acknowledgement

The authors would like to thank Mr. T. Koyanagi and Mr. K. Kiriya for their assistance with the simulation studies. Also, one of the authors, Alper Akdag, acknowledges Japanese Government for financial support during his stay, with the Monbusho scholarship.

(Manuscript received January 25, 2000, revised July 3, 2000)

References

1. T.J.E. Miller, Reactive Power Control in Electric Systems, A Wiley-Interscience Publication, 1982
2. M. Mohaddes, A.M. Gole, P.G. McLaren, "A Neural Network Controlled Optimal Pulse-Width Modulated STATCOM", IEEE Trans. on Power Delivery, Vol. 14, No. 2, pp. 481-488, April 1999
3. F.Z. Peng, J.S. Lai, J.W. McKeever, J. VanCoevering, "A Multilevel Voltage-Source Inverter with Separate DC Source for Static VAR Generation", IEEE. Trans. on Industry Applications, Vol. 32, No. 5, pp. 1130-1137, Sept/Oct. 1996
4. G. Joos, L. Moran, P. Ziogas, "Performance Analysis of a PWM Inverter VAR Compensator", IEEE Trans. on Power Electronics, Vol. 6, No. 3, pp. 380-391, July 1991
5. C. Schauder, M. Mehta, "Vector Analysis and Control of Advanced Static VAR Compensators", IEE Proc.-C, Vol. 140, No. 4, pp. 299-306, July 1993
6. B. M. Han, G.G. Karady, J.K. Park, Si.I Moon, "Interaction Analysis Model for Transmission Static Compensator with EMTP", IEEE Trans. on Power Delivery, Vol. 13, No.4, pp. 1297-1302, Oct. 1998
7. H. Akagi, Y. Kanazawa, A. Nabae, "Instantaneous Reactive Power Compensators Comprising Switching Devices without Energy Storage Components", IEEE Trans. on Industry Applications, Vol. IA-20, No. 3, pp. 625-630, May/June. 1984
8. K. Suzuki, M. Yajima, M. Nohara, S. Ueda, H. Sato, Y. Eguchi, "Control Method 50MVA Self- Commutated Static VAR Compensator", T.IEE Japan, Vol. 117-B, No. 7, pp. 953-959, 1997 (in Japanese)
9. K. Suzuki, T. Nakajima, H. Konishi, T. Nakamura, "A Study of Control System for Self Commutated Converter Compensator" T. IEE Japan, Vol. 112-B, No.1, pp. 67-73, 1992 (in Japanese)
10. S. Mori, K. Matsuno, M. Takeda, M. Seto, "Development of a Large Static VAR Generator Using Self Commutated Inverters for Improving Power System Stability", IEEE Trans. on Power Systems, Vol.8, No. 1, pp.371-377, Feb. 1993

11. N. Eguchi, M. Yamamoto, S. Konishi, T. Morita, "Control System for Self-Commutated Static VAR Compensators with Unbalanced Load Compensation" T. IEE Japan, Vol.114-D, No.4, pp.444-450, 1994 (in Japanese)
12. A. Campos, G. Joos, P. Ziogas, J. Lindsay, "Analysis and Design of a Series Voltage Compensator for Three-Phase Unbalanced Sources", IEEE Trans. on Industrial Electronics, Vol. 39, No.2, pp. 159-167, Apr. 1992
13. C. Hochgraf, R.H. Lasseter, "Statcom Controls for Operation with Unbalanced Voltages", IEEE Trans. on Power Delivery, Vol. 13, No.2, pp. 538-544, Apr. 1998

Appendix A

Transformation of the equation in (2), from stationary α-β frame to the rotating d-q frame can be obtained as follows:

$$\begin{bmatrix}\alpha\\ \beta\end{bmatrix}=[C]\begin{bmatrix}d\\ q\end{bmatrix} \quad \text{.....(A1)}$$

where $[C]=\begin{bmatrix}\cos(\omega t) & -\sin(\omega t)\\ \sin(\omega t) & \cos(\omega t)\end{bmatrix}$

$$\begin{bmatrix}V_{s\alpha}\\ V_{s\beta}\end{bmatrix}=\begin{bmatrix}L\dfrac{di_\alpha}{dt}\\ L\dfrac{di_\beta}{dt}\end{bmatrix}+\begin{bmatrix}V_{i\alpha}\\ V_{i\beta}\end{bmatrix} \quad \text{.....(A2)}$$

$$[C]\begin{bmatrix}V_{sd}\\ V_{sq}\end{bmatrix}=L\frac{d}{dt}\left([C]\begin{bmatrix}i_d\\ i_q\end{bmatrix}\right)+[C]\begin{bmatrix}V_{id}\\ V_{iq}\end{bmatrix} \quad \text{...(A3)}$$

$$\begin{bmatrix}V_{sd}\\ V_{sq}\end{bmatrix}=[C]^{-1}L\frac{d}{dt}\left([C]\begin{bmatrix}i_d\\ i_q\end{bmatrix}\right)+\begin{bmatrix}V_{id}\\ V_{iq}\end{bmatrix} \quad \text{.....(A4)}$$

$$\begin{bmatrix}V_{sd}\\ V_{sq}\end{bmatrix}=L\frac{d}{dt}\left(\begin{bmatrix}i_d\\ i_q\end{bmatrix}\right)+[C]^{-1}L\begin{bmatrix}i_d\\ i_q\end{bmatrix}\frac{d}{dt}\left(\begin{bmatrix}\cos(\omega t) & -\sin(\omega t)\\ \sin(\omega t) & \cos(\omega t)\end{bmatrix}\right)+\begin{bmatrix}V_{id}\\ V_{iq}\end{bmatrix} \quad \text{.....(A5)}$$

$$\begin{bmatrix}V_{sd}\\ V_{sq}\end{bmatrix}=\begin{bmatrix}L\dfrac{di_d}{dt}\\ L\dfrac{di_q}{dt}\end{bmatrix}+\omega L\begin{bmatrix}0 & -1\\ 1 & 0\end{bmatrix}\begin{bmatrix}i_d\\ i_q\end{bmatrix}+\begin{bmatrix}V_{id}\\ V_{iq}\end{bmatrix} \quad \text{.....(A6)}$$

Appendix B

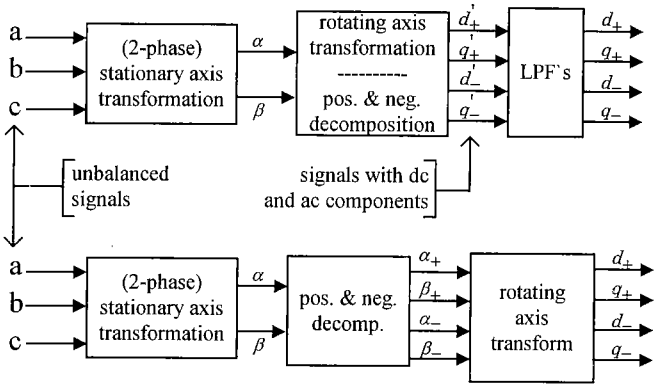

Fig. A1. Basic principles of the positive and negative sequence decomposition (a) in d-q frame (b) in α-β

Alper Akdağ (Student Member) received the B.Sc. and M.Sc. degrees in electrical engineering from Middle East Technical University, Ankara, Turkey, in 1993 and 1996, respectively. He is currently working towards the Ph.D. degree at Chiba Institute of Technology, Chiba, Japan. Between 1993-1997, he was a Research Assistant in the Electrical and Electronics Engineering Department, Middle East Technical University, and also a part time researcher in the Power Electronics Division, TUBITAK Information Technologies and Electronics Research Institute.
Mr. Akdag is a student member of IEEE and the Institute of Electrical Engineers of Japan.

Susumu Tadakuma (Member) was born in Kumamoto, Japan, on February 5, 1939. He received the B.Sc. and Dr. of Engineering Degrees from Waseda University, Tokyo, Japan, in 1962 and 1978, respectively. He joined Toshiba Corporation in 1962, where he was engaged in power electronics applications to industrial motor drives and high speed transport systems at R&D Center (1962-1978) and Heavy Apparatus Engineering Laboratory (1979-1994). Since 1995 he has been a Professor of Chiba Institute of Technology, Chiba, Japan. Dr. Tadakuma is a Fellow, IEEE and a member of IEEJ and SICE, Japan. He served as a Member at Large, IAS Executive Board, IEEE from 1994 to 1997 and Chairman of the IEEE Industry Applications Society Tokyo Chapter from 1995 to 1996.

Hideaki Minakata (Member) received the M.S. and the Ph.D. degrees in electrical engineering from University of Tokyo in 1994 and 1997, respectively. He is a Lecturer with the Department of electrical engineering, Chiba Institute of Technology, Japan. His current research interests are in the areas of control theory, power drive systems and humanoid robots.