# Synthesis and analysis of a discrete-time CNN using 1-dimensional cell circuits with S stable points (S = 2, 3, 4, ...)

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In this paper, a discrete-time CNN using 1-dimensional cell circuits with S stable points ( $S=2,3,4,\ldots$ ) is proposed. The circuit structure and the behavior of the proposed CNN is simple by exploiting discrete-time 1-dimensional circuits as the cell circuits. Since the proposed cell circuit takes as much as S of states, the proposed CNN can demonstrate the multiple-valued traveling wave phenomena. Furthermore, the proposed cell circuit is suitable for integration thanks to the circuit design by using switched-current (SI) techniques. The computer simulations are performed concerning a 2-dimensional CNN which is constructed with the proposed cell circuits. The 1-dimensional cell circuit with S stable points is designed by a standard CMOS process. Furthermore, the proposed cell circuit is built with commercially-available IC's. The experimental result is in close agreement with the simulation result. The proposed CNN is integrable by a standard CMOS technology.

Keywords: cellular neural networks, traveling waves, switched current, discrete-time circuits, analog circuits

## 1. Introduction

Recently, the CNNs (Cellular Neural Networks) using chaos circuits attract many researchers' attension. In these CNN, traveling waves can be observed. The traveling wave is one of the most frequently encountered phenomena in the study of natural phenomena in physics and biology [1],[2]. The CNN using chaos circuits opens up new vistas for application systems, for example, models for the transport phenomena in biological and physical systems, shortest-path finding systems, and so on [1]-[7]. For this reason, many researcher's have shown prototypes of the CNN using chaos circuits [3]-[5]. These CNNs exploit Chua's chaos circuits [8]-[10] as the cell circuits. Since the cell circuits used in these CNNs have two stable points,  $P_{-}$ and  $P_+$ , the CNNs employing Chua's chaos circuits can demonstrate binary-valued traveling wave phenomena. However, the circuit structure and the chaotic behavior of Chua's circuit are very complicated since it is a 3-dimensional continuous-time chaos circuit. In the design of the CNNs, the simplicity of the behavior as well as the circuit structure are important. Being distinct from such features, hardware-implementation of the CNN with a standard IC technology is favorable. This feature will enable the CNNs to get into experimental tools for the large scale networks.

In this paper, a discrete-time CNN using 1-dimensional cell circuits with S stable points (S =

 $2,3,4,\ldots$ ) is proposed. The circuit structure and the behavior of the proposed CNN is simple by exploiting discrete-time 1-dimensional circuits as the cell circuits. The proposed CNN can demonstrate the multiple-valued traveling wave phenomena since the proposed cell circuit takes as much as S of states. Furthermore, the proposed cell circuit synthesized using switched-current (SI) techniques [11],[12] is suitable for integration since 1. SI circuits can be implemented by a standard digital process, 2. they exhibit low sensitivity to both temperature variations and supply voltage variations, and 3. they are more robust than volage-mode counterparts against the reduction of the supply voltages.

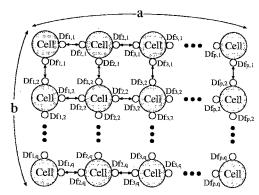


Fig.1 Circuit architecture of the discrete-time CNN which consists of 1-dimensional cell circuits with S stable points  $(S=2,3,4,\ldots)$ .

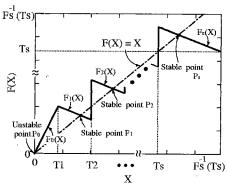


Fig.2 Nonlinear function of the proposed cell circuit.

The computer simulations are performed concerning a 2-dimensional CNN which is constructed with the proposed cell circuits. Furthermore, the proposed cell circuit is built with commercially-available IC's.

### 2. Architecture

Figure 1 shows the circuit architecture of the proposed CNN. The proposed CNN consists of  $a \times b$  cells. In Fig.1, Df<sub>i,j</sub> is a non-negative diffusion coefficient. The dynamics of the proposed CNN is based on the following equation:

$$\begin{split} X_{i,j}(t+1) &= FC(X_{i,j}(t)) \\ &= F(X_{i,j}(t)) + Q, \ \cdots \cdots (1) \end{split}$$

where

$$\begin{split} Q &= Df_{i,j-1}(t_d) \ X_{i,j-1}(t) + Df_{i,j+1}(t_d) \ X_{i,j+1}(t) \\ &+ Df_{i-1,j}(t_d) \ X_{i-1,j}(t) + Df_{i+1,j}(t_d) \ X_{i+1,j}(t) \end{split}$$

and

$$\mathrm{Df}_{\mathrm{i},\mathrm{j}}(\mathrm{t_d}) = \left\{ \begin{array}{ll} \mathrm{D}_{\mathrm{i},\mathrm{j}} & \quad \mathrm{if} \quad \mathrm{t_d} = q\mathrm{t}, \\ 0 & \quad \mathrm{if} \quad \mathrm{t_d} \neq q\mathrm{t}. \end{array} \right.$$

In Eq.(1),  $X_{i,j}(\cdot)$  is a positive variable,  $F(\cdot)$  and  $FC(\cdot)$  are piecewise-linear functions which have S stable points  $(S=2,3,4,\ldots)$ ,  $D_{i,j}$  is a positive constant, and q is an integer parameter. Figure 2 shows an example of the nonlinear function when  $t_d \neq qt$ . The nonlinear function  $F(\cdot)$  in Eq.(1) is given by the following condition:

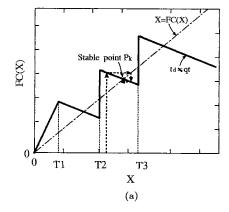
$$F(X) = F_0(X) + F_1(X) + \cdots + F_S(X)$$

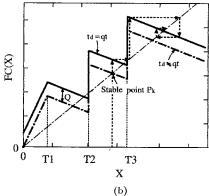
$$(X \in [0, F_S^{-1}(T_S))), \cdots (2)$$

where  $F_n(X)$  (n = 0, 1, ..., S) is the linear function on the interval  $[T_n, T_{n+1})$ . The linear function  $F_n(X)$  satisfies the following conditions:

$$T_0 = 0$$
 and  $T_{S+1} = F_S^{-1}(T_S)$   
and  $F_n(T_n) < T_{n+1}$   
and  $\left| \frac{dF_n(X)}{dX} \right| < 1.$  (3)

In Fig.2,  $P_0$  is an unstable point and  $P_k$ 's (k = 1, ..., S) are stable points. The stable point,  $P_k$  (k = 1, ..., S), satisfies the following condition:





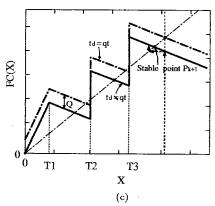


Fig.3 An example of the traveling process. (a) Stable point of FC(·). (b) Stable point when  $t_d=qt$ . (c) Stable point when  $t_d\neq qt$ .

$$P_k = FC(P_k)$$
  $(k = 1, \dots, S)$ .  $\dots \dots \dots (4)$ 

When the nonlinear function satisfies

$$FC(T_k) < T_{k+1}, \cdots (5)$$

the basin [5],[6] of the stable point  $P_k$  (k = 1, ..., S) is given by the following equations:

$$B(P_1) = (0, T_2),$$
  
 $B(P_2) = [T_2, T_3),$   
...  
 $B(P_S) = [T_S, T_{S+1}).$  (6)

These equations mean that the state of the i, j-th cell will settle down to  $P_k$  when  $X \in [T_k, T_{k+1})$ . When  $t_d \neq qt$ , the state of the cell cannot transfer to the other states since the nonlinear function satisfies the conditions of Eqs.(3) and (5) (see Fig.3 (a)). On the

other hand, the state of the cell can transfer from  $P_k$  to the higher state (see Fig.3 (b)) when

$$\begin{aligned} & & \text{t}_{\mathrm{d}} = q \mathrm{t} \\ \text{and} & & & \mathrm{F}_k(\mathrm{T}_k) + \mathrm{Q} < \mathrm{T}_{S+1} \\ \text{and} & & & & \mathrm{F}_k(\mathrm{T}_k) + \mathrm{Q} \geq \mathrm{T}_{k+1}. \quad \cdots \qquad (7) \end{aligned}$$

The parameter Q for the i,j-th cell is determined by the diffusion coefficient  $Df_{i,j}(t_d)$  and the states of the neighbor cells,  $X_{i-1,j}(t)$ ,  $X_{i+1,j}(t)$ ,  $X_{i,j-1}(t)$ , and  $X_{i,j+1}(t)^{\dagger}$ . From. Eqs.(6) and (7), the proposed cell can take as much as S of states. After the state of the cell transfered from  $P_k$  to the higher state, the state of the cell settles down to around  $P_l$  (l > k) by closing the connection of the cell (see Fig.3 (c)). When  $t_d \neq qt$ , the variable  $X_{i,j}(t)$  is mapped q-1 times by  $FC(\cdot)^{\dagger\dagger}$ . Hence, the state of the cell is affected by the parameter q.

The validity of the circuit algorithm will be confirmed in Sect.4.

# 3. Circuit Structure

Figure 4 shows the proposed cell circuit designed by using SI techniques. The synthesis of this circuit is based on the following equation:

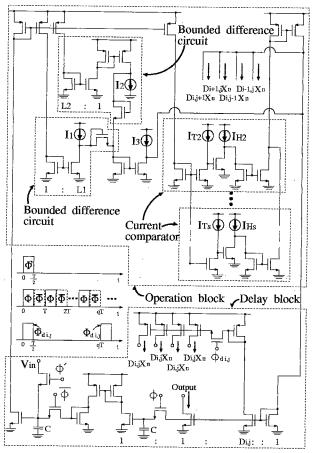


Fig.4 SI cell circuit with S stable points  $(S=1,2,3,\ldots)$ .

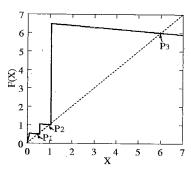


Fig.5 Nonlinear function of the proposed cell obtained by numerical simulation.

$$\begin{split} X_{i,j}(t+1) &= I_3 - \{ (I_1 \ominus L1X_{i,j}(t)) + (X_{i,j}(t)/L2 \ominus I_2) \} \\ &+ u(X_{i,j}(t) - I_{T2}) \cdot I_{H2} + \dots + u(X_{i,j}(t) - I_{Ts}) \cdot I_{Hs} \\ &+ Df_{i,j-1}(t_d) \ X_{i,j-1}(t) + Df_{i,j+1}(t_d) \ X_{i,j+1}(t) \\ &+ Df_{i-1,j}(t_d) \ X_{i-1,j}(t) + Df_{i+1,j}(t_d) \ X_{i+1,j}(t), \quad (8) \end{split}$$

where  $u(\cdot)$  is the unit step function and  $\ominus$  is the bounded-difference operator defined as

$$\alpha \ominus \beta \stackrel{\Delta}{=} \left\{ \begin{array}{cc} \alpha - \beta & (\alpha > \beta), \\ 0 & (\alpha \leq \beta). \end{array} \right. \cdots (9)$$

Different from the circuit proposed in [11], the proposed cell has S stable points and cannot generate chaotic signals without the effect of the other cells. In Fig.4, the operations,  $(I_1 \ominus L1X(t))$  and  $(X(t)/L2 \ominus I_2)$ , are realized by the bounded-difference circuits composed of the current mirrors and the diode-connected MOSFET's. The parameters, L1 and L2, are realized by the currentcopying ratios in the bounded-difference circuits. The operation,  $u(\cdot)$ , is realized by the current comparator composed of the CMOS inverters and the current mirrors. The delay block is the SI track & hold circuit [11]. In the delay block, the diffusion coefficients, D<sub>i,j</sub>'s, are realized by the current-copying ratios. By setting the gate bias  $\phi_{\text{di,j}}$  to 0, the proposed SI cell circuit can close the connection of the i, j-th cell. Therefore,  $\phi_{\rm di,j}=0$ corresponds to  $Df_{i,j}(t_d) = 0$ . The output of the operation block is delayed by one cycle and it is fed back to the input terminal of the operation block. The initial value  $X_{i,j}(0)$  of this circuit is given by  $V_{in}$  in the delay block. The operations of the switches,  $\phi$ ,  $\bar{\phi}$ ,  $\phi'$ , and  $\phi_{\rm di,j}$ , are set to as shown in Fig.4. Here, the period of  $\phi_{\text{di,j}}$  corresponds to the parameter q.

## 4. Simulation

To confirm the validity of the circuit design, numerical simulations are performed regarding to the circuit algorithm. The dynamics of the simulated CNN is based on the following equations:

$$X_{i,j}(t+1) =$$

<sup>&</sup>lt;sup>†</sup>As Fig.3 (b) shows, the state of the cell transfers to the higher state since the position of the stable point  $P_k$  is moved by the effect of the other cells, Q.

<sup>&</sup>lt;sup>††</sup>From Eqs.(1)  $\sim$  (3), the state of the i,j-th cell settles down around  $P_l$  (l>k) by setting  $q\gg 1$ .

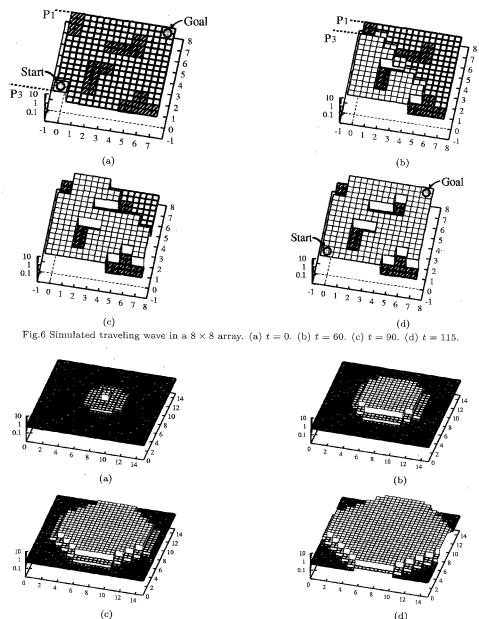


Fig.7 Simulated traveling wave in a  $16 \times 16$  array. (a) t = 0. (b) t = 15. (c) t = 35. (d) t = 55.

$$\begin{cases} 5.4X_{i,j}(t) \\ +Df_{i,j-1}(t_{d}) & X_{i,j-1}(t) + Df_{i,j+1}(t_{d}) & X_{i,j+1}(t) \\ +Df_{i-1,j}(t_{d}) & X_{i-1,j}(t) + Df_{i+1,j}(t_{d}) & X_{i+1,j}(t) \\ & (0 \le X_{i,j}(t) < 0.1), \\ -0.1X_{i,j}(t) + 0.55 \\ +Df_{i,j-1}(t_{d}) & X_{i,j-1}(t) + Df_{i,j+1}(t_{d}) & X_{i,j+1}(t) \\ +Df_{i-1,j}(t_{d}) & X_{i-1,j}(t) + Df_{i+1,j}(t_{d}) & X_{i+1,j}(t) \\ & (0.1 \le X_{i,j}(t) < 0.55), \end{cases}$$

$$-0.1X_{i,j}(t) + 1.1 \\ +Df_{i,j-1}(t_{d}) & X_{i,j-1}(t) + Df_{i,j+1}(t_{d}) & X_{i,j+1}(t) \\ +Df_{i-1,j}(t_{d}) & X_{i-1,j}(t) + Df_{i+1,j}(t_{d}) & X_{i+1,j}(t) \\ & (0.55 \le X_{i,j}(t) < 1.05), \end{cases}$$

$$-0.1X_{i,j}(t) + 6.6 \\ +Df_{i,j-1}(t_{d}) & X_{i,j-1}(t) + Df_{i,j+1}(t_{d}) & X_{i,j+1}(t) \\ +Df_{i-1,j}(t_{d}) & X_{i-1,j}(t) + Df_{i+1,j}(t_{d}) & X_{i+1,j}(t) \\ & +Df_{i-1,j}(t_{d}) & X_{i-1,j}(t) + Df_{i+1,j}(t_{d}) & X_{i+1,j}(t) \\ & & (1.05 \le X_{i,j}(t) < 55.5). \end{cases}$$

The proposed cell in the simulated CNN has three stable points. Hence, the proposed cell in the simulated

CNN has as much as three of states. The basin of the stable point,  $P_k$   $(k=1,\ldots,3)$ , is given by the following equations:

In the numerical simulations, the parameter q for  $\phi_{\rm di,j}$  (see in Fig.4) was set to 5.

Figure 5 shows the simulated nonlinear function of the proposed cell. Figure 6 shows the traveling wave in a  $8\times 8$  array of the proposed cells. In Fig.6, the hatched cells are the obstacles created by setting the diffusion coefficients to 0. The diffusion coefficients of the non-hatched cells,  $D_{i,j}$ 's, were set to 0.02. In Fig.6, the *Goal* cell has switched from  $P_1$  to  $P_3$  after 115 cycles. Figure 7 shows the traveling wave in a  $16\times 16$  array of the proposed cells. In numerical simulations

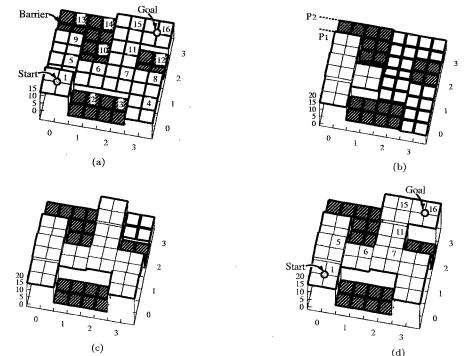


Fig.10 Simulated traveling wave in a  $4 \times 4$  array. (a) t = 20ms. (b) t = 40ms. (c) t = 70ms. (d) t = 100ms.

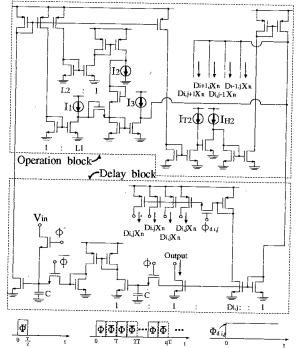


Fig.8 SI cell circuit used in SPICE simulations.

of Fig.7, the diffusion coefficients of all cells were set to 0.02. As Fig.7 shows, the multiple-valued traveling wave phenomena such as a ripple mark can be modeled by the proposed CNN.

In Figs.6 and 7, the characteristics of the proposed CNN were analyzed by numerical simulations. However, the non-ideal effects of the circuit implementation such as the clock feedthrough, finite output resistance of the tarnsistors, etc. cannot be analyzed by this method. Therefore, to analyze those non-ideal effects and to con-

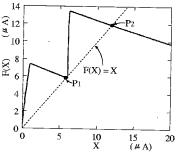


Fig.9 Nonlinear function of the proposed cell circuit obtained by SPICE simulation.

firm the validity of the above-mentioned simplification, the SPICE simulations [13] are performed regarding to a  $4\times 4$  array of the proposed cell circuits. To save space, only the SPICE simulation results concerning the proposed cell circuit with two stable points will be given. The proposed cell circuit is designed by assuming a standard CMOS process.

Figure 8 shows the SI cell circuit used in SPICE simulations. SPICE simulations were performed under the conditions that  $V_{\rm dd}=5V$ ,  $I_1=6\mu A$ ,  $I_2=0.4\mu A$ ,  $I_3=6\mu A$ ,  $I_{T2}=6\mu A$ ,  $I_{H2}=6\mu A$ ,  $I_1=6$ ,  $I_1=$ 

$$B(P_1) = (0\mu A, 6\mu A),$$

$$B(P_2) = [6\mu A, 30\mu A).$$

Figure 10 shows the traveling wave in a  $4 \times 4$  array of the proposed cell circuits. In the SPICE simulation of Fig.10, the initial state of the 1st cell was set to  $P_2$  and the initial states of all the other cells were set to  $P_1$ .

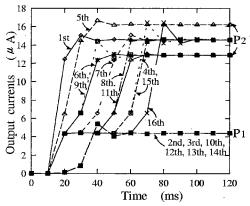
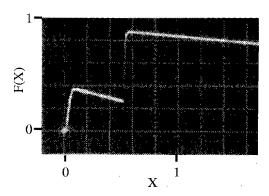


Fig.11 States of the cell circuits obtained by SPICE simulation.



Hori.: 0.2 V/div., Ver.: 0.2 V/div.

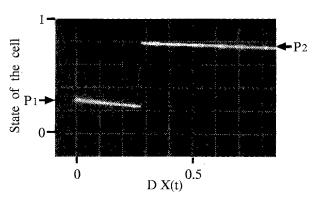
Fig.12 Measured nonlinear function in the experimental circuit.

In Fig.10, the hatched cells are the obstacles created by setting  $\phi_{\rm di,j}$  to 0 V. The parameter  $\phi_{\rm di,j}$  of the non-hatched cell was set to 5 V.  $^{\dagger}$  Thus, the proposed circuit can control the initial state of the CNN, electronically. Figure 11 shows the states of the cell circuits obtained by the SPICE simulations. From Figs.10 and 11, the traveling wave has propagated to the 16th cell after 100  $\mu s$ .

## 5. Experiment

To analyze the non-ideal effects of the proposed cell circuit, the experiments concerning the nonlinear function and the state of the cell circuit are perfomed regarding to the experimental circuit. The experimental circuit was built with commercially available IC's, 4007UB and 4528B, and discrete bipolar transistors, 2SC1815 and 2SA1085. The IC's 4528B were used to generate the clock pulses,  $\phi$  and  $\overline{\phi}$ , in the delay block. The discrete bipolar transistors were used to realize the current sources. And the value of the capacitor C was set to 10 nF.

Figure 12 shows the nonlinear function of the experimental circuit. Figure 12 is in close agreement with the simulated result in Fig.9. Figure 13 shows the state of the proposed cell in the experimental circuit. The experimental circuit was operated with a clock frequency equal to 100 Hz. In Fig.13, the state, P<sub>1</sub>, of the cell cir-



Hori.: 0.1 V/div., Ver.: 0.2 V/div.

Fig.13 Measured state of the proposed cell in the experimental circuit.

Table 1 Comparison.		
	Proposed	V.Pérez-Muñuzuri
	model	et al.'s model
Implementation	Current-mode	Voltage-mode
method	analog circuit	analog circuit
Type of		
output signals	Discrete-time	Continuous-time
Dimension of		
cell circuit	1-dimension	3-dimensions
Type of		
traveling wave	Multiple-value	Binary-value

cuit has switched to  $P_2$  when the external bias DX(t) is  $0.28\ V.$ 

#### 6. Discussion

In the past, several types of CNNs using chaos circuits have been proposed. Among others, V.Pérez-Muñuzuri et al. adopted Chua's chaos circuit to realize CNN using chaos circuit [5],[6]. This CNN employing Chua's chaos circuits can demonstrate binary-valued traveling wave phenomena. The cell circuit of this CNN is a 3-dimensional continuous-time choas circuit designed by voltage-mode techniques.

On the other hand, the advantages of the proposed method are as follows: 1. The circuit structure and the behavior of the proposed CNN is simple by exploiting discrete-time 1-dimensional circuits as the cell circuits. 2. Since the proposed cell circuit takes as much as S of states, the proposed CNN can demonstrate the multiple-valued traveling wave phenomena. 3. The proposed cell circuit synthesized using switched-current (SI) techniques is suitable for integration since a) SI circuits can be implemented by a standard digital process, b) they exhibit low sensitivity to both temperature variations and supply voltage variations, and c) they are more robust than volage-mode counterparts against the reduction of the supply voltages.

Table 1 shows the comparison of the above mentioned methods.

## 7. Conclusion

A discrete-time CNN using 1-dimensional cell circuits with S stable points ( $S=2,3,4,\ldots$ ) has been proposed in this paper.

The numerical simulations showed that the proposed CNN can demonstrate the multiple-valued traveling

 $<sup>^\</sup>dagger Since$  the cell circuit used in SPICE simulations has 2 stable points, the parameter  $\phi_{\rm di,j}$  of the non-hatched cell was fixed to 5 V

wave phenomena. The SPICE simulations concerning a  $4 \times 4$  array of the proposed cell circuits showed that the proposed CNN can search the shortest-path after 100  $\mu$ s. The experiment of the breadboard circuit was in close agreement with the simulation result. The proposed CNN is integrable by a standard CMOS technology.

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### References

- (1) S.C.Muller, T.Plesser, and B.Hess, "Two-dimensional spectrophotometry of spiral wave propagaiton in the Belousov-Zhabotinskii reaction I. Experiments and digital representation. II. Geometric and kinematic parameters," physica, vol.D24, no.4, pp.71-96, March 1987.
- (2) R.R.Klevecz, J.Bolen, and O.Durán, "Self-organization in biological tissues: Analysis of asynchronous and synchronous periodicity, turbulence and synchronous chaos emergent in coupled chaotic array," Int. J. Bifurc. and Chaos, vol.2, no.4, pp.941-953, March 1992.
- V.Pérez-Muñuzuri, V.Pérez-Villar, and L.O.Chua, "Traveling wave front and its failure in a one-dimensional array of Chua's circuits," J. Circuits & Syst., and Comput., vol.3, no.3, pp.211-215, March 1993.
- V.Pérez-Muñuzuri, V.Pérez-Villar, and L.O.Chua, "Autowaves for image processing on a two-dimensional CNN array of excitable nonlinear circuits: flat and wrinkled labyrinths,' IEEE Trans. Circuits & Syst., vol.40, no.3, pp.174-181, March
- (5) L.Pivka, "Autowaves and spatio-temporal chaos in CNNspart I: a tutorial," IEEE Trans. Circuits & Syst., vol.42, no.10, pp.638-649, Oct. 1995.
- (6) L.Pivka, "Autowaves and spatio-temporal chaos in CNNspart II: a tutorial," IEEE Trans. Circuits & Syst., vol.42, no.10, pp.650-664, Oct. 1995.
- (7) L.Nemes and T.Roska, "A CNN model of oscillation and chaos in ant colonies: a case study," IEEE Trans. Circuits & Syst., vol.42, no.10, pp.741-745, Oct. 1995.
- J.M.Cruz and L.O.Chua, "An IC chip of Chua's circuit," IEEE Trans. Circuits & Syst., vol.40, no.10, pp.614-626, Oct.
- K.Murali and M.Lakshmanan, "Effect of sinusoidal excitation on the Chua's circuit," IEEE Trans. Circuits & Syst., vol.39, no.4, pp.264-270, April 1992.
- J.M.Cruz and L.O.Chua, "A CMOS IC nonlinear resistor for Chua's circuit," IEEE Trans. Circuits & Syst., vol.39, no.12, pp.985-995, Dec. 1992.
- (11) Takahiro Inoue, Kyoko Tsukano, Kei Eguchi, "Synthesis and Analysis of Chaotic Circuits Using Switched-Current Techniques," IEICE Transactions on Fundamentals, Vol.E79-A, No.6, pp.758-763, Jun. 1996.
- (12) M.Degaldo-Restituo, F.Medeiro, and A.Rodriguez-Vázquez, "Nonlinear switched-current CMOS IC for random signal generation," Electron. Lett., vol.29, no.25, pp.2190-2191, Dec.
- (13) PSpice user's guide, MicroSim Corporation, 1989.

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