Paper

Control Aspects of a Transformerless Five Level Cascaded Inverter Based Single Phase Photovoltaic System

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A single phase transformerless five level cascaded inverter based grid connected photovoltaic system is discussed in this paper. By avoiding the transformer, advantages such as high efficiency and low embodied energy are achieved. The implementation of the cascaded topology allows for reduced AC filter effort, firstly by generating a five level voltage waveform and secondly by achieving minimum switching frequencies by using its switch state redundancies. Control aspects described in this paper are the switching scheme and the grid current control method. A digital implementation and first experimental results of a multi carrier PWM voltage controller showing the effectiveness of the switching scheme are presented.

Key words: Grid connected photovoltaic system, multi level inverter, current control, PWM voltage control

1. Introduction

In the past, various different inverter topologies have been suggested, or are currently used, for low power, single phase, grid connected photovoltaic (PV) systems (see Fig. 1). A common technology is a switch mode, full bridge inverter in combination with a line frequency transformer. The transformer, however, is (in most countries) not a requirement and inverters without transformers offer several advantages. A recent European market survey [1] shows, that transformerless inverters outperform those with transformers with respect to higher efficiency, lower cost, weight, and embodied energy (see Table).

Besides advantageous transformerless concepts, multi level inverters promise good solutions, since these inverters have the ability of producing "stepped" output voltage waveforms, which approach the sinusoidal waveform better than waveforms produced by conventional full bridge inverters. Multi level inverters therefore require less filter effort on the AC side, which makes the inverter cheaper, lighter and more compact. In order to generate the "multi level" (stepped) output voltage waveform, different DC voltage levels are necessary, which can be provided by dividing a PV array in appropriate sections.

Table I. Comparison of 16 Switch Mode Inverters for Single Phase, Grid Connected PV Systems (European Manufacturers) in the 1.5-2.5 kW Power Range [1].

Inverter Type	Number	η_{max} (%)	Weight (kg/kW)	Price (US$/W)
With Transformer	10	93.7	15.3	0.88
Transformerless	6	95.3	9.1	0.60

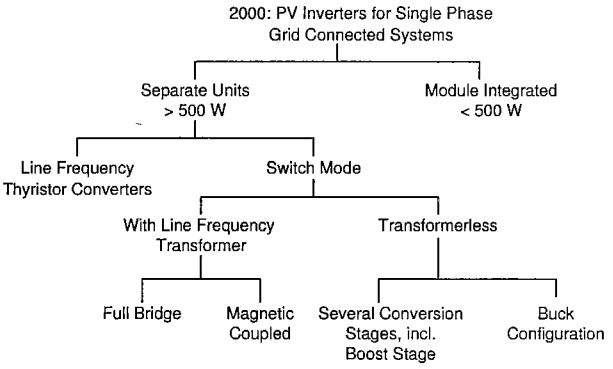

Figure 1. Different commercially available photovoltaic inverter topologies for single phase grid connected systems (< 6 kW) in 2000 (German market) [1].

The suitability of a five level cascaded inverter for a transformerless single phase grid connected PV system is currently investigated and a 1.92 kW prototype system is under development. The objectives of this paper are:

- To describe the prototype system and its control,
- to present simulation results of a dual ramptime current control method, and
- to present experimental results of the open loop, voltage controlled operation of the system.

The paper is organised as follows: Section 2 describes the prototype system, its control structure for the grid connected application and the applied switching scheme. Section 3 discusses the dual ramptime current control method and presents simulation results. Section 4 presents experimental results which have been obtained from the

implementation of a multi carrier PWM control scheme. Finally, the digital realisation of the open loop voltage control and the switching scheme is described.

2. System Description

Fig. 2 gives an overview of the proposed system for a grid connected application. It consists of two PV arrays with the same current and voltage rating, the cascaded inverter, the system control, an AC filter (here shown simplified as a single inductor L_{inv}) and the AC grid represented by a voltage source. The cascaded inverter is comprised of two conventional single phase full bridge topologies with their AC outputs connected in series. Each bridge can create three different voltage levels at its AC output allowing for an overall five level AC output voltage (an example voltage waveform is shown in Fig. 3b)).

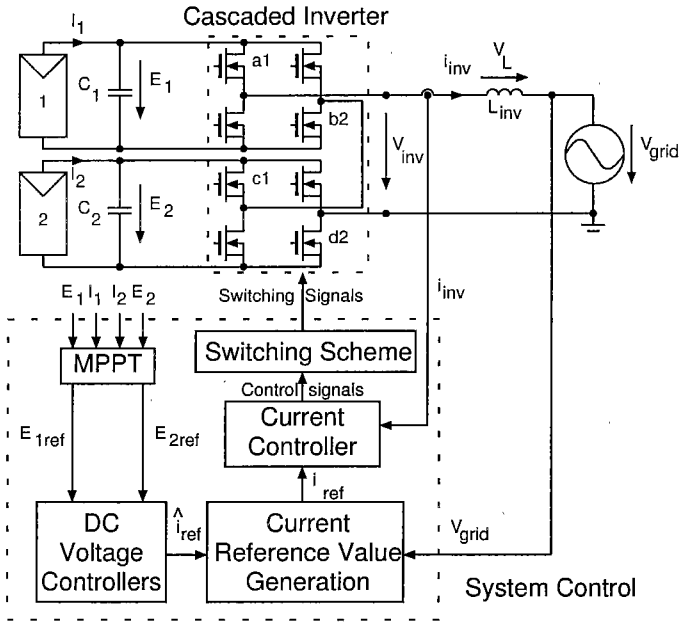

Figure 2. Proposed grid connected photovoltaic system with a five level cascaded inverter.

Due to the step down nature of the topology high DC bus voltages are necessary to ensure power flow from the two PV arrays to the grid. The system can only operate when the sum of the DC bus voltages $E_1 + E_2$ is greater than the amplitude of the grid voltage at all times (e.g. $\hat{v}_{gridmax} \approx$ 373 V for a 240 V system). This constraint determines the minimum power rating of the system. Many crystalline PV modules available on the market today have 36 cells in series and operating voltages of approximately 17 V at 25 °C and 1000 W/m^2. However, when the temperature increases, the operating voltage can drop to as low as 12 V per module. Due to this behaviour, at least 14 crystalline 36-cell-PV modules in series are required for each of the two PV arrays, allowing for system power ratings of 1.3 kW and above.

The system control includes a Maximum Power Point Tracker (MPPT), DC bus voltage controllers, the current reference value generation, the current controller and the switching scheme. Its main tasks are the maximisation of the energy transferred from the PV arrays to the grid, and the generation of a sinusoidal current, i_{inv}, with minimum harmonic distortion.

The MPPT uses an algorithm [2], which is based on the fact, that in single phase systems the instantaneous power oscillates at twice the line frequency. The oscillation of the AC power also causes a ripple on the DC voltage and DC power of the PV array. Where other MPPT algorithms impose forced perturbations on the system in order to find the MPP (and with that create additional losses), this algorithm uses the naturally occurring perturbations for the tracking process. It is described in more detail in [3] and [4], and will not be discussed further in this paper.

Both PV arrays can be tracked individually in order to minimise mismatch losses. Two DC voltage controllers ensure stable operation under changing insolation conditions. Due to the individual control of the DC bus voltages, E_1 and E_2 may be different, which has implications on the current control as will be described in Section 3.

2.1 The Switching Scheme

The five level cascaded inverter in Fig. 2 has 16 states which allow bi-directional current flow at a fixed inverter output voltage. When assuming $E_1 = E_2 = E$, six of these states generate an inverter output voltage of $v_{inv} = 0$, four states generate $v_{inv} = E$, four states generate $v_{inv} = -E$, one state generates $v_{inv} = 2 \cdot E$, and one state generates $v_{inv} = -2 \cdot E$. Using the given redundancies, a cyclic switching sequence with the following characteristics based on work presented in [5] has been developed [6]:

- The switching frequency of each switch is minimal. To achieve this, one objective when choosing the switching sequence is to keep switches on as long as possible.
- Each switch should be stressed in the same way in order to achieve equal losses in each switch and with that an equal temperature distribution within the inverter.
- The voltages E_1 and E_2 are used alternately in successive ripple current periods.
- The ripple in the DC bus capacitors should be minimal since this causes losses and increases cost.
- The two zero states where the two PV array voltages cancel each other out are avoided.

Fig. 3 shows simulation results of a simple, low frequency, voltage control scheme which has been implemented for preliminary tests of the prototype system (it will be described in more detail in section 4). Fig. 3b) shows the inverter output voltage v_{inv} on a p.u. basis. The carrier frequency of 2 kHz is reflected in the voltage pulses of the five level waveform. Figs. 3c)-f) show the gate signals for the four full bridge legs. By employing the above mentioned switching scheme, the switching frequency is reduced by a factor of four in comparison with the carrier frequency (the "effective switching frequency", which is relevant for the filter design).

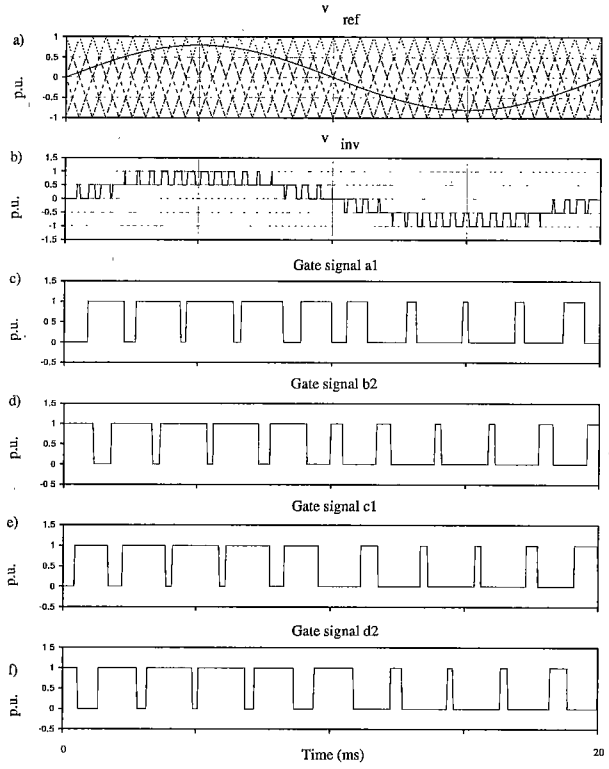

Figure 3. Simulation results for the multi carrier PWM control scheme and the switching scheme. a) Alternative Phase Opposition Disposition (APOD) multi carrier PWM scheme [7], b) inverter output voltage v_{inv}, c)-f) gate signals for switches a1, b2, c1 and d2 (see Fig. 2.)

3. Dual Ramptime Current Control

For grid connected operation, the inverter output current is controlled using the *dual ramptime* current control method [8, 9, 10]. This control method is an adaptation of ramptime current control [10, 12, 11].

With ramptime current control, each and every switching instant is chosen to occur a determined period of time after each zero crossing of the current error signal. Furthermore, that time is determined with the intent that the next zero crossing of the current error signal will occur one half the target ripple current period after the previous current error signal zero crossing.

The basic principles of these methods will be briefly explained with the help of Figs. 4-7. The current error signal i_{err} is put through a comparator to produce a binary current error polarity signal. This signal is used solely to indicate the instants in time when the current error signal crosses zero. The controller causes each switching instant to occur a calculated amount of time after each zero crossing of the current error signal. The calculation attempts to generate each switching instant so that the total time the current error signal remains on one side of zero is half the desired ripple current period. The controller uses the timings of previous switching instants and current error zero crossings in the algorithm (see Fig. 4).

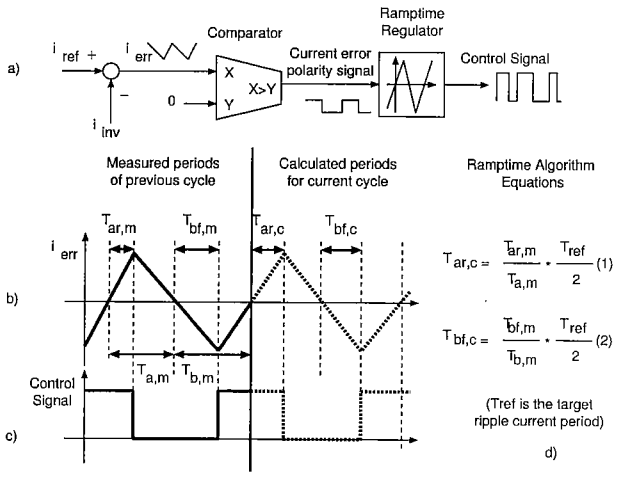

Figure 4. a) Principle of the ramptime control method, b) current error i_{err} with indicated measured (index m) and to be calculated (index c) periods, c) control signal, d) equations to determine $T_{ar,c}$ and $T_{bf,c}$.

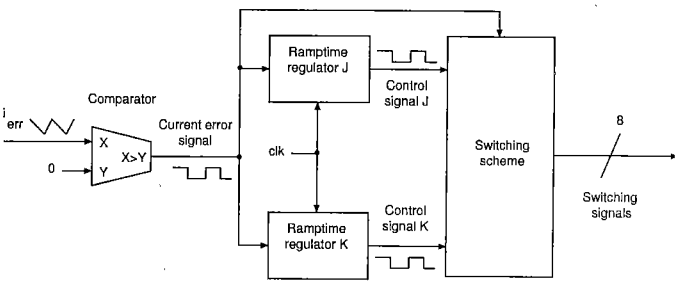

Figure 5. Dual ramptime current control.

Dual ramptime current control is an adaptation of ramptime current control used to provide full controllability of the current while minimising the ripple current in multi-level inverters. For a detailed description, please refer to the references [8, 9, 10]. As shown in Fig. 5, two ramptime regulators are used together to control the AC current. Most of the time, one ramptime regulator is used, controlling the current by providing switching between two adjacent voltage levels as shown in Fig. 6.

If and when the time since the last zero crossing of the current error signal exceeds a set maximum (which is just larger than half the target ripple current period), the second ramptime regulator is switched on. The transition from single regulator operation to dual regulator operation is shown in more detail in Fig. 7 for the transition from single J regulator operation to dual J and K regulator operation in the first half of the positive halfwave (indicated in Fig. 6). First the J regulator is operating on its own. When the current error signal is not returning to zero at the expected time this is used as an indication that the slope of the current error signal is approaching zero, and therefore requiring the dual ramptime operation to maintain controllability. At this time the K regulator is turned on and its control signal is immediately set "high" (so that the next voltage level is chosen). The current error signal then begins ramping rapidly towards zero, and soon crosses

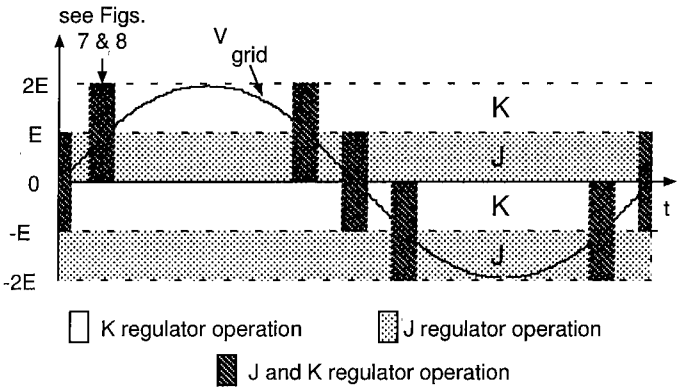

Figure 6. J and K regulator operating areas.

zero. Then, the K ramptime regulator sets its control signal back to "low" (so that the voltage level with a low current error signal slope is chosen) a short fixed period of time after the zero crossing, returning the current error signal to the same slope (and the converter to the same voltage level) as when the K regulator was originally turned on. Thereafter, the two ramptime regulators continue to operate concurrently, each generating a low duty cycle output which is set "high" for short periods to bring the current error signal rapidly across zero. The two regulators essentially operate anti-synchronised. Within each regulator, the "low" to "high" transition is determined using the normal ramptime algorithm, while the "high" to "low" transition is determined as a short fixed period of time after the zero crossing.

The current error signal crossing zero before the output of the respective regulator has been set "high" is used as an indication that the slope of the current error signal has increased sufficiently for operation with one regulator alone to be feasible. In this example, when the early current error signal zero crossing occurs, the J regulator is turned off, and operation continues with the K regulator operating alone.

Fig. 8 displays the inverter output current and voltage as well as the gate signals for switches a1, b2, c1 and d2 during the chosen example period indicated in Fig. 6. During the dual regulator operation three voltage levels need to be accessed which leads to an increase in switching frequency.

The operation of the five level inverter using dual ramptime control is simulated for the case where the two PV array voltages, E_1 and E_2, are not equal. With normalized AC voltage and current (V_{inv}=1 p.u., I_{inv}=1 p.u.) and a target ripple current frequency of 20 kHz, a 0.01 p.u. impedance filter inductor is used (31.8 μH, f=50 Hz). E_1 and E_2 are used alternately in successive ripple current periods. The PV arrays provide only real power and the PV array voltages are chosen to E_1=0.741 p.u. and E_2=0.819 p.u.

The current error, line current and inverter output voltage over one line cycle are shown in Fig. 10. These waveforms are expanded in Fig. 9 where 2 milliseconds of operation

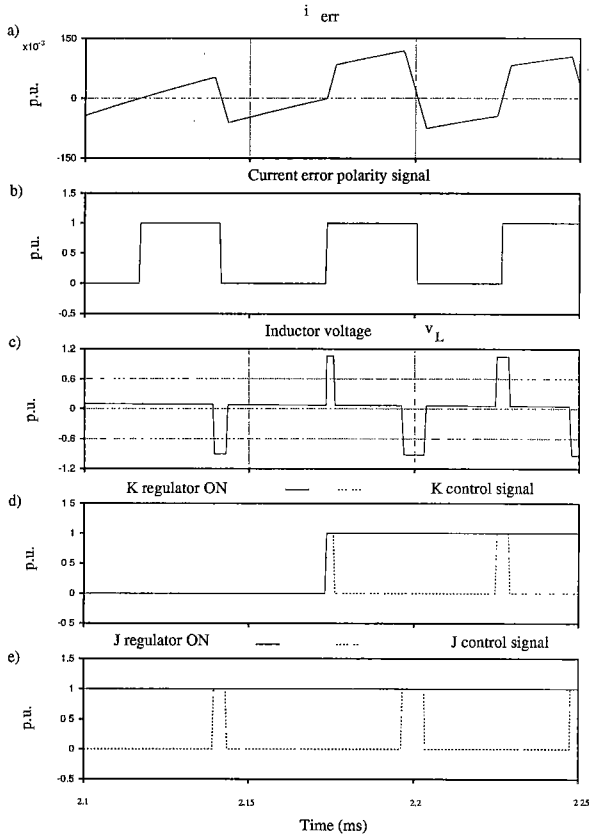

Figure 7. Transition from single to dual regulator operation, a) current error i_{err}, b) current error polarity signal, c) inductor voltage v_L, d) K regulator ON signal and K regulator control signal, e) J regulator ON signal and J regulator control signal.

around a voltage level transition are shown. The dual ramptime operation can be seen between the 1.6 and 2.0 milliseconds time points. The effect of the alternating voltage across the filter inductance in successive ripple current periods is apparent in the current waveforms. The alternating voltage causes some disruption, but the current error signal is kept close to zero. The line current harmonics spectrum is shown in Fig. 11. The low order harmonics are kept below -55 dB, and the ripple current frequency is within a narrow controlled band. Due to the selected switching scheme a harmonic component at half the ripple current frequency is present. Also, although the switching scheme still cycles through the switch states during the transition periods, the switching frequency increases and the ratio of ripple current frequency to switching frequency of 4/1 can no longer be maintained during these periods.

4. Experimental Results

To test the system, an open loop voltage controller has been realised, which operates the cascaded inverter at a low switching frequency (500 Hz). The implemented voltage control method is a multi carrier PWM method. The principle of this method is shown in Fig. 3a): The reference is sampled through four triangular carrier waveforms displaced by half the reference waveform

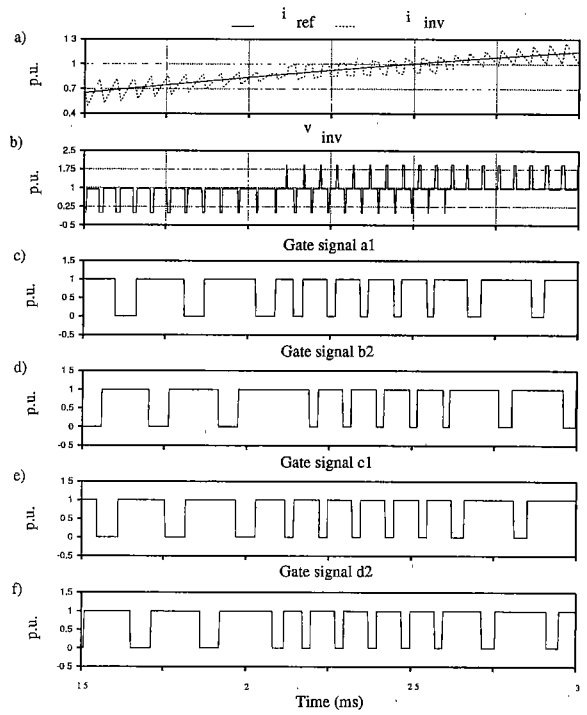

Figure 8. Dual regulator operation, a) inverter output current, i_{inv}, and reference current, i_{ref}, b) inverter output voltage v_{inv}, c) - f) gate signals for a1, b2, c1 and d2.

amplitude. The phases of the four carriers are displaced from each other by 180 degrees alternately (Alternative Phase Opposition Disposition, APOD) [7].

Due to ease of reconfiguration, better repeatability and higher noise immunity, the method has been implemented digitally using an field programmable gate array (Altera EPF6016) and a PIC16C73A processor. A structural overview of the control board is given in Fig. 12. The FPGA additionally includes the state machine of the cyclic switching sequence described in section 2.1 and the dead time generation.

The digital implementation of the APOD PWM method and the dead time generation is based on work presented in [13]. For the APOD PWM, due to the symmetry of the carrier and reference waveforms, only one halfwave and two carriers have to be considered.

Fig. 13 displays the generation of the PWM signal $PWM1$ (active between 0 and 0.5 p.u. of v_{inv}) through comparison of the reference value, its complement and an up counter c and *or* logic. The PWM signal $PWM2$ (active between 0.5 and 1 p.u of v_{inv}) is generated similarly by using the complement of the up counter (=down counter) and *and* logic (see Fig. 14).

The reference value is sampled 8 times per carrier period and forms a stepped waveform as shown in Fig. 13. It is therefore possible, that multiple edges are detected during the rising edge or falling edge of the carrier. Additional logic ensures that only one edge is accepted for each rising or falling edge of the carrier.

The PWM signals form the input to a state machine

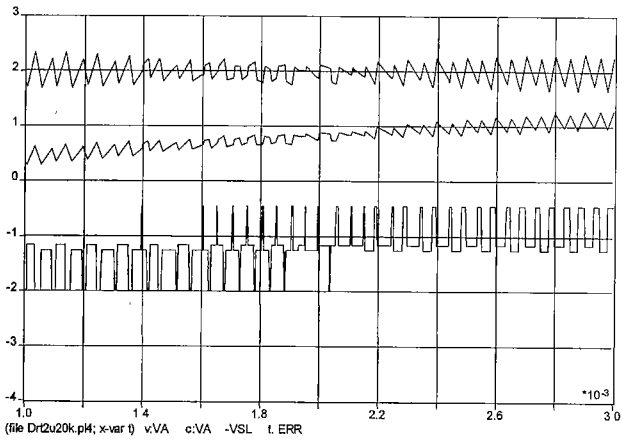

Figure 9. Transition simulated results, $E_1 \neq E_2$, top: current error (offset +2), middle: inverter output current i_{inv}, bottom: inverter output voltage, v_{inv} (offset -2).

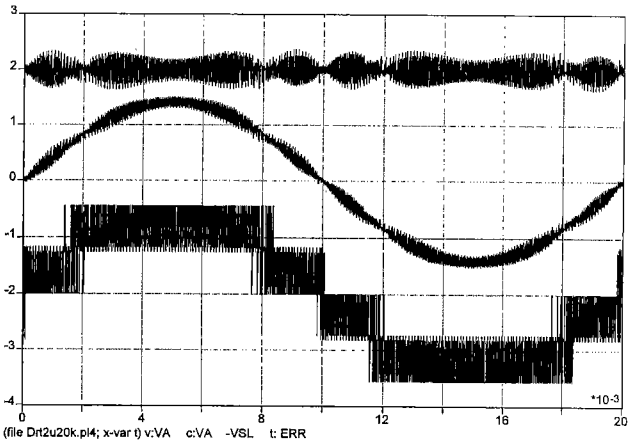

Figure 10. Line cycle simulated results, $E_1 \neq E_2$, top: current error (offset +2), middle: inverter output current i_{inv}, bottom: inverter output voltage, v_{inv} (offset -2).

which realises the cyclic switching sequence. The dead times are generated by using shift registers. Figs. 15 and 16 show experimental results obtained with two 30 V DC power supplies on the DC busses and an inductive-resistive load ($R = 111.1\ \Omega$, $L_{inv} = 33.74$ mH). The recordings show the five level voltage waveform, the "apparent" switching frequency of 2 kHz and the factor four lower frequency of the gate signals.

5. Conclusions

A transformerless five level cascaded inverter based grid connected PV system and its control are presented in this paper. System control aspects such as the switching scheme and the current control method are described. The switching scheme uses the switch state redundancies of the inverter so that the switching frequency is minimised, the switches are stressed equally, and the PV arrays are loaded alternately.

Due to the desirable individual tracking of the two PV arrays, the current control method has to ensure controllability of the inverter output current under different

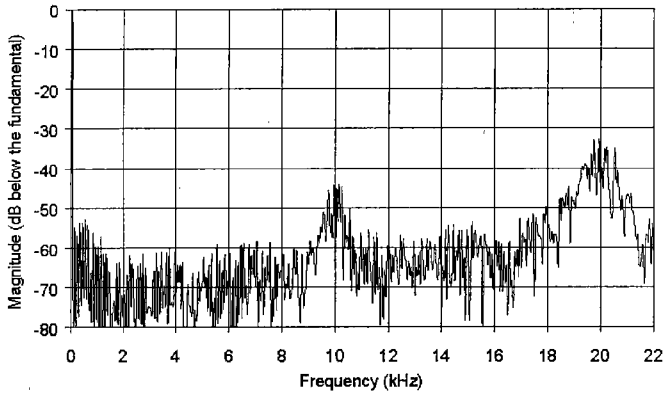

Figure 11. Spectrum of inverter output current i_{inv}, $E_1 \neq E_2$.

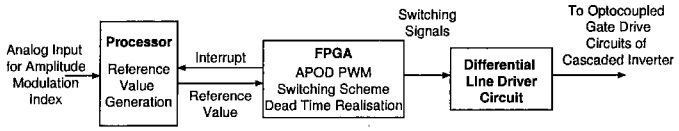

Figure 12. Structure of the open loop voltage control board.

PV array voltages. The simulation results presented show that the application of the dual ramptime control method results in a fully controllable current in the five level inverter with 10% difference in voltage between the arrays.

Experimental results are presented for a preliminary open loop voltage control of the system. The digital realisation of the multi carrier PWM method is described and results are presented which show the effectiveness of the switching scheme: the switching frequency is a quarter of the ripple current frequency and the switches are stressed equally.

Further work will include the implementation of the MPPT and the dual ramptime current control method. Also investigations are necessary to analyse and solve the negative influence of earth leakage currents on the system performance.

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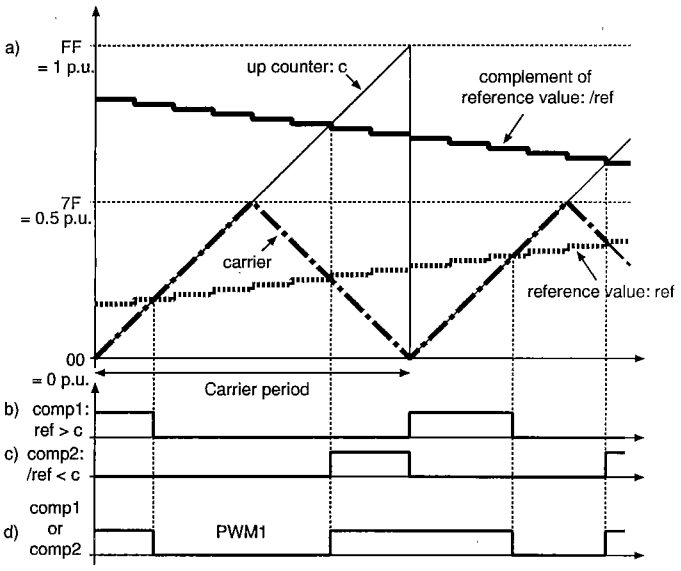

Figure 13. Digital realisation of APOD PWM, example of carrier/reference value comparison. a) An eight bit up counter c is used to "generate" the carrier. It is compared b) with the reference value ref and c) its complement $/ref$. Both comparator outputs combined d) generate the PWM signal for the carrier.

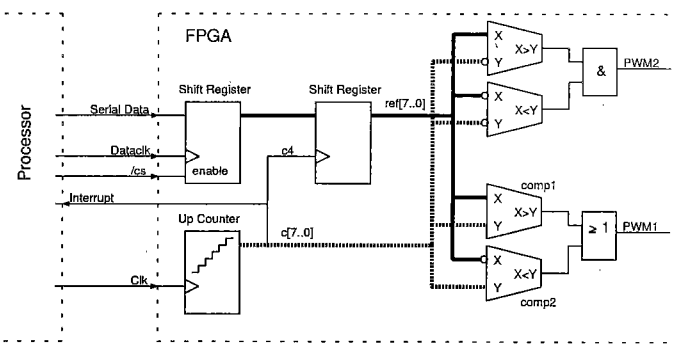

Figure 14. Block diagram of the digital APOD PWM realisation.

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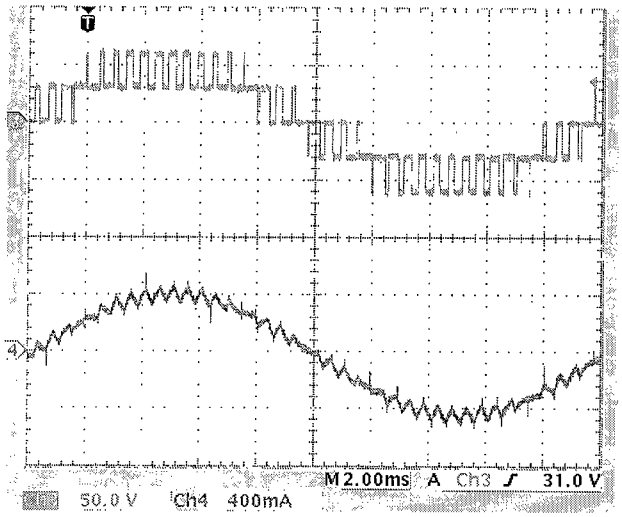

Figure 15. Experimental results, Ch3: inverter output voltage v_{inv}, Ch4: inverter output current i_{inv}.

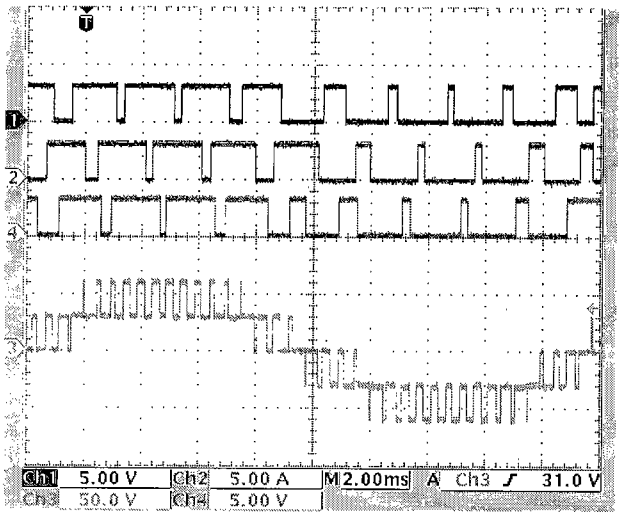

Figure 16. Experimental results, Ch1: Gate signal a1, Ch2: Gate signal b2, Ch4: Gate signal c1, Ch3: Inverter output voltage v_{inv}.

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