Paper

On the Switching Surge in the Current Resonant Inverter for the Induction Furnace Application

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Abstract:

Surges are undesirable with respect to both the reliability and the efficiency of power devices. This study presents the mechanism of surge occurrence in an induction heating power supply. A 2 kW full bridge series resonant inverter based on zero-voltage-switching (ZVS) and phase-locked loop (PLL) control is used as a power supply. In this inverter, the modified PLL does not only keep the output current and the voltage in phase but also makes the system operate in ZVS mode. When the PLL mismatches the resonant frequency in a manner of current phase lead, the inverter operates at the non-ZVS mode and the surge voltage heavily affects the switching elements to an extent mainly decided by the recovery energy of the drain-source diode in the power devices. In order to solve this problem, this paper proposes a modified PLL to be the phase error zero.

Key words: Induction Heating, Phase-locked Loop, Power Device, Resonant Circuit, Surge, Zero Voltage Switching

1. Introduction

Induction heating is an electrical method of heating metals or conductive materials for processes such as melting, surface hardening, brazing, soldering, welding, tempering and annealing, forming and extrusion, shrink fitting, and others. Normally when it is utilized as surface hardening, in accordance with skin effect, higher operating frequency makes energy concentrate at thinner surface of the work. Therefore it can efficiently heat the work surface in a very short time and with minimal energy.

Recent development of power devices has brought about a wide use of switching operation in the field of power conversion because of high efficiency. The voltage-fed inverter has become a standard topology for high power converters in induction heating. Previously a series resonant circuit has been proposed to solve the problems of low efficiency at high frequency power supply [1][2][3][4]. However, to design a high operating frequency induction heating power supply, there remain some serious problems as follows.

(1) MOSFET devices are popularly used as power components of high frequency power supply. The parasitic capacitor between the drain and source of MOSFET generates a very high switching loss in a high frequency operation condition. It exhausts much energy and reduces the life of power devices.

(2) Surges happening at power device cause a very high voltage stress, heat and high frequency noise. They often deteriorate power devices and make a serious electro-magnetic interference (EMI) problem. So it is undesirable with respect to the reliability, electro- magnetic interference and efficiency of power devices.

(3) During the heating process, the load resistance and inductance vary hugely. This variation changes the resonant frequency of the resonant circuit since the load inductance and resistance are part of a resonant tank. In order to get the maximum output energy, operating frequency of power supply must track the resonant frequency of resonant tank

In this study, a modified PLL controlled inverter is first proposed such that the changing resonant frequency of the equivalent load can be tracked and meanwhile to keep the ZVS condition.

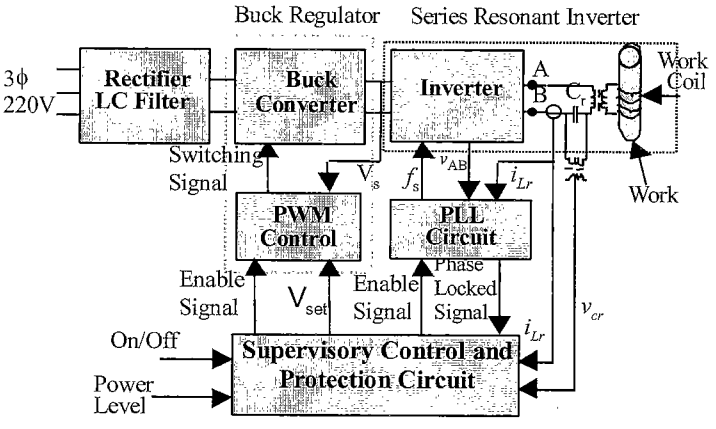


Fig. 1. System structure of the proposed power supply

This study also clarifies the surge generation mechanism.

As surge is normally a very high frequency noise, it was difficult to understand its behavior, and it bothered electronic engineers very much, especially in high frequency switching power supply. There have been many papers studied in this topic [5][6][7][8]. However, they didn't clarify the surge generation mechanism completely. In this study, it is discovered that the surge in the non-ZVS mode is quite larger than in the ZVS mode. The non-ZVS mode is caused by a mismatching of the PLL control, which occurs especially when the work reaches the Curie temperature, and the operating frequency exceeds its limit of PLL circuit. At the non-ZVS mode, the surge appears in the power devices very huge, sometimes damages them.

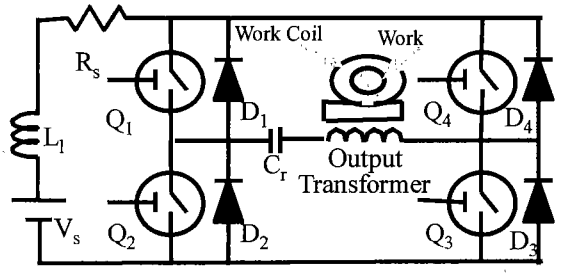


Fig. 2. Power stage circuit diagram

2. System Description

A PLL controlled voltage-fed series-resonant inverter operating at switching frequency 100 kHz and output power 2 kW is used as the power supply for an induction heating system (Fig. 1). The system includes 4 parts: buck regulator, PLL circuit, inverter and supervisory control & protection. The buck regulator regulates the output power where the amplitude of the output voltage is controlled. The PLL circuit is used to control the output frequency to match the resonant frequency of the output circuit, so that the output current and voltage are in phase to maintain maximum output power.

The PLL circuit further ensures that the system operates in ZVS mode. The supervisory control and protection circuit monitors the output current and voltage stress on the resonant capacitor Cr, and offers a soft start function. A full bridge inverter based on MOSFET is used. Input power of the system can be single phase or three-phase 220V.

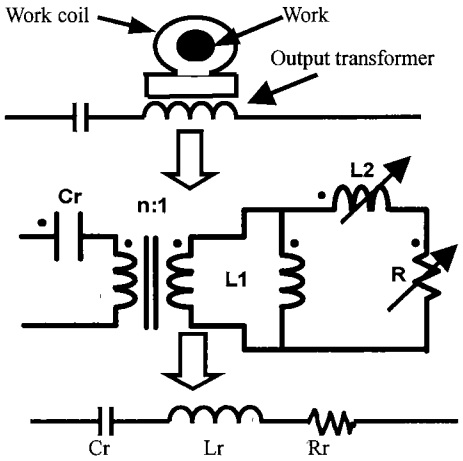


Fig. 3. Equivalent circuit of work, work coil in the primary side of output transformer

A full bridge inverter is designed to supply power to work shown as Fig. 2. The output resonant equivalent circuits constructed by output capacitor, output transformer, work coil and work (Fig. 3). In Fig. 3, L2 and R are equivalent inductance and resistance of work and work coil, the value of L2 and R is varied in the heating process.

3. The Principle of Modified PLL

Normally the PLL circuit is taken to trace of the resonant frequency to make output voltage and output current in phase, output power is usually kept in a maximum condition [9]. In this paper the modified PLL circuit not only keeps tracking of the resonant frequency but also makes system work in ZVS mode, where surges are minimized.

The modified PLL control circuit is shown as Fig. 4. A type-4 phase detector (RCA CD4046)[10] is applied in this system. It is independent of the duty-cycle ratio of the waveforms and exhibits a marked sensitivity to frequency for even the smallest offset. This circuit is therefore often referred to as a phase/frequency detector.

In Fig. 3, the impedance Z of the resonant tank SRC (Series Resonant Circuit) circuit and the current angle can be calculated as follows.

$\omega = 2\pi f_S$, f_S : switching frequency of

$$= R_r\sqrt{1+Q_0^2(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega})}\angle\phi_i = Z_r\angle\phi_i \quad (1)$$

$$\phi_i = \tan^{-1} Q_0(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}) \quad (2)$$

where $Q_0 = \frac{\omega_0 L_r}{R_r}$, $\omega_0 = \frac{1}{\sqrt{L_r C_r}}$

Suppose phase difference $|(\omega-\omega_0)/\omega_0| << 1$, the phase angle can be simplified as

$$\phi_i \cong 2Q_0\frac{\Delta\omega}{\omega_0} \quad (3)$$

$\Delta\omega = \omega - \omega_0$

$\omega = 2\pi f_S$, f_S : switching frequency of v_{AB}

The fundamental wave of the input voltage v_{AB} of the resonant tank circuit as shown in Fig. 4(a) can be found from Fourier analysis as follows.

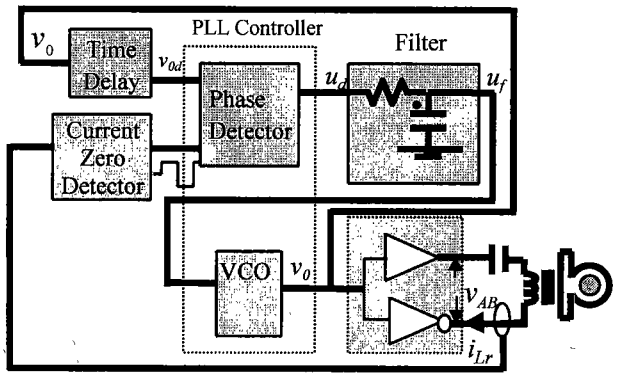
$$v_{AB1} = \frac{2V_S}{\pi}\sin\omega t \quad \text{for } 0 < \omega t \le 2\pi \quad (4)$$

The load current through the resonant tank circuit can be expressed as

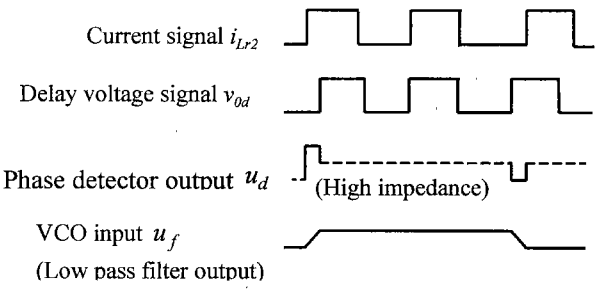
$$i_{Lr} = \frac{v_{AB1}}{Z} = \frac{2V_s}{\pi Z_r}\sin(\omega t - \phi_i) \quad (5)$$

The phase difference ϕ_i between the voltage v_{AB1} and load current i_{Lr} is obtained by Eq. (1). In Fig. 4 (a), the output signal v_0, which is alternately on and off with a duty ratio of 50 %, of VCO is amplified by inverter and put on the

resonant tank. The induced load current i_{Lr1} is changed to square wave i_{Lr2} after current zero detector, and this square wave is sent to phase detector to compare with output voltage delay signal v_{0d}. u_d is the average output voltage of phase detector. u_f is given by integrator of u_d is sent to VCO. Phase detector and filter in Fig. 4 (a) organize the integrator of phase error. In no phase error period, the output of phase detector is in a high impedance condition shown as Fig. 4 (b), so the phase error is integrated by filter.



(a)



(b)

Fig. 4. (a) Block diagram of modified PLL
(b) The time chart of PLL

Time delay circuit is constructed by first order RC circuit which determines the voltage phase delay. Since the output signal of VCO is a square wave and the delay time T_d is the rise time of output signal of the filter from zero voltage to the threshold voltage of phase detector, the delay time is constant in different frequency conditions. The output voltage delay phase $\phi_{VD}(t)$, consequently, becomes as follows.

$$\phi_{VD}(t) = T_d\omega(t) \qquad (6)$$

In the steady state, the phase angle between output current and voltage is equal to $\phi_{VD}(t)$.

The detailed operation of the proposed PLL control block can be explained as follows:

At the beginning, the inverter is disabled and the frequency of VCO is f_{min}. There is no current flowing in the series resonant circuit. No i_{Lr2} signal sends to the phase detector. According to Eq. (6), the output voltage delay angle ϕ_{VD} is always greater than zero. Thus the phase detector output u_d(t) remains in positive and high impedance. Since the input signal u_f(t) of VCO is the integration of u_d(t), the output frequency of VCO increases from f_{min} to f_{max} according to the VCO characteristic shown in Fig. 5.

When the inverter is enabled, current starts to flow in the series resonant circuit. The phase angle and the magnitude of the induced current can be derived by Eqs. (2) and (5). As the phase angle ϕ_i at the switching frequency f_{max} is greater than the delay angle ϕ_{VD}, the phase detector output u_d (t) is negative value and the integrator output u_f(t) decreases. The oscillating frequency of VCO accordingly decreases. This condition will continue until the next equation is satisfied.

$$\phi_{VD}(t) = \phi_i(t) \qquad (7)$$

When $\phi_{VD}(t) = \phi_i(t)$, the integrator output u_f(t) remains unchanged and the oscillating frequency of VCO will be fixed. This concept can be illustrated by Fig. 6.

From Fig. 6, two design principles can be derived. First, at the time t0 when enable signal is first applied to the inverter, the phase angle ϕ_i should be greater than the delay angle ϕ_{VD} to ensure the phase detector output u_d(t) negative, which implies that the oscillating frequency will decrease from the frequency f_{max} toward f_{min}. Second, the decline slope of phase angle ϕ_i vs. ω should be greater than the decline slope of delay angle ϕ_{VD} vs. ω to ensure a stabilized

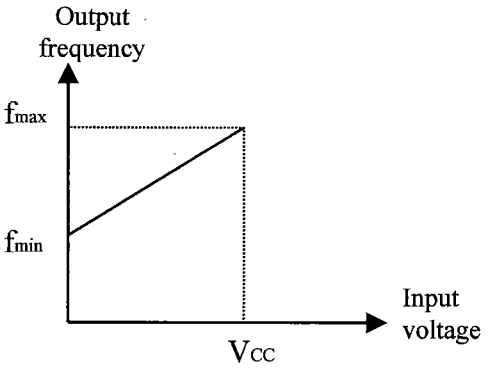


Fig. 5. Input voltage vs. output frequency (VCO)

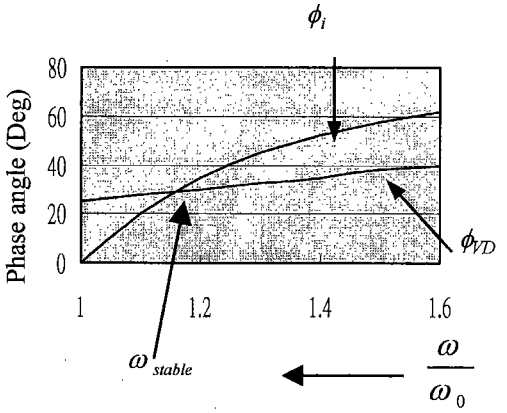


Fig. 6. The relation between current phase ϕ_i, voltage delay phase ϕ_{VD} and operating frequency

$$(T_d = 1\mu S, L_r = 260\,\mu H, C_r = 20nS, \omega_0 = \frac{1}{\sqrt{L_r C_r}})$$

operation frequency f_{stable} could be reached. These two constraints can be represented in mathematical forms:

$$\frac{2Q_0}{\omega_0}\omega_{\max} - 2Q_0 > T_d\omega_{\max} \quad (8)$$

Where $\omega_{\max} = 2\pi f_{\max}$ and $\frac{2Q_0}{\omega_0} > T_d$

If the design principles are met, the oscillating frequency of VCO will be

$$\omega_{stable} = \frac{2Q_0}{2Q_0 - T_d\omega_0}\omega_0 \quad (9)$$

which is greater than ω_0. If $\frac{2Q}{\omega_0}$ is higher than T_d, the phase of current lags behind the inverter voltage for a certain degree which is proportional to T_d. This means that the phase angle of the output current can be controlled by adjusting delay time T_d, and the inverter will be operated in a ZVS mode in steady state.

According to the block diagram of the modified PLL system in the time domain shown in Fig. 7, the mathematical model of modified PLL is obtained as Fig.8. This model allows us to analysis the error phase $\Phi_e(s)$ as follows.

The definition of variables:

Kd: the gain of phase detector

$F(s) = \frac{K_F}{s}$ = The Laplace transform of integrator

KF: the gain of integrator

Kv: the gain of VCO

KI=1 = the gain of inverter

$K_Z = \frac{2Q_0}{\omega_0}$ = The gain of resonant tank (SRC)

$\Omega(s)$: The Laplace transform of $\omega_1(t)$

From Fig. 8, we get Eqs. (10) and (11). Here we consider the response of error phase ϕ_e against the step change of ϕ_{stable}.

$$\Phi_i(s) = \frac{K_d F(s) K_V K_I K_Z}{1 + K_d F(s) K_V K_I K_Z}\Phi_{stable}(s) \quad (10)$$

The Laplace transform of error phase $\phi_e(t)$ becomes

$$\Phi_e(s) = \Phi_{stable}(s) - \Phi_i(s) = \frac{1}{1 + K_d F(s) K_V K_I K_Z}\Phi_{stable}(s) \quad (11)$$

For the step change of ϕ_{stable}, we have

$\phi_{stable}(t) = u(t)\Delta\Phi$

where $\Delta\Phi$ is the amplitude of the step change ϕ_{stable}.

From the Laplace transform of this equation, we have

$$\Phi_{stable}(s) = \frac{\Delta\Phi}{s} \quad (12)$$

By substituting Eq. (12) to Eq. (11), we get

$$\Phi_e(s) = \frac{1}{1 + K_d F(s) K_V K_I K_Z} \bullet \frac{\Delta\Phi}{s} \quad (13)$$

In the steady state condition,

$$\phi_e(\infty) = \lim_{s\to 0} s\Phi_e(s) = \lim_{s\to 0} s \bullet \frac{1}{1 + K_d F(s) K_V K_I K_Z} \bullet \frac{\Delta\Phi}{s}$$

$$= \frac{\Delta\Phi}{1 + K_d F(s) K_V K_I K_Z} = 0 \quad (14)$$

because of F (0)=∞.

It is evident from the Eq. (14) that the steady-state phase error is locked to be zero with the modified PLL. This result has been verified by the experiment.

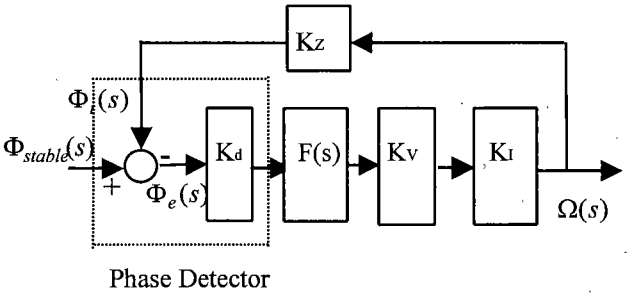


Fig. 8. The mathematical model of modified PLL

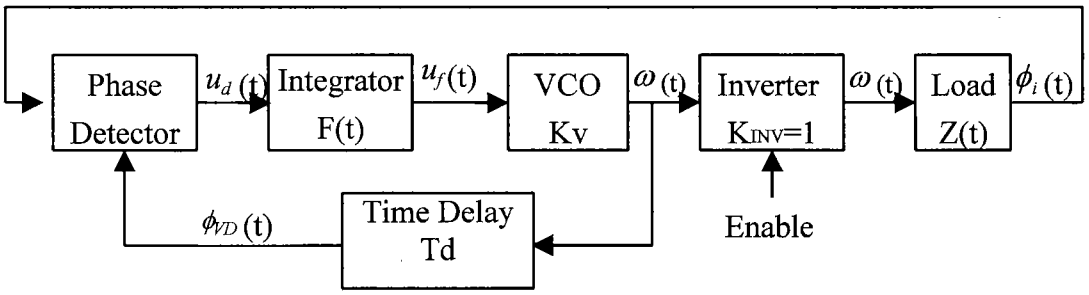


Fig. 7. Block diagram of the PLL system in the time domain

4. Surge Analysis of the ZVS Mode

As far as the proposed application is considered, the switching frequency of the inverter lies in the range of 60 k to 120 kHz and the dominant surge frequency is centered around 6 MHz approximately. To obtain a practical model for the corresponding surge analysis, it is required the model be as simple as possible and meanwhile be accurate enough to be able to simulate the observed phenomenon.

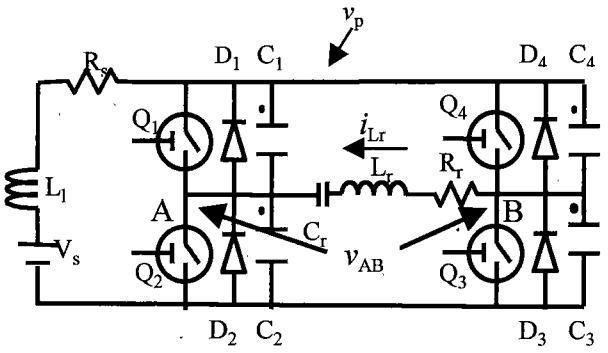


Fig. 9. Power stage equivalent circuit

Fig.9 shows the proposed equivalent circuit model for analyzing the surge phenomenon. In Fig.3, the equivalent series $R_rL_rC_r$ circuit representing the electrical load of the heating system referred to the primary side [9]. Due to the very high surge frequency, the prestages of the resonant inverter can be simply modeled as a DC voltage source of V_s in series with equivalent source impedance, namely L_l in series with R_s. Finally, each of the four MOSFET switches is modeled as an idea switch together with its corresponding non-ideal body diode and the junction capacitance. It is worth pointing out here that inclusion of the non-ideal diode to take into account the reverse recovering current effect is very essential to model the observed surge phenomenon [10][11].

In this section, the surge phenomenon is first analyzed for the ZVS mode. In other words, the switching frequency is a little higher than the resonant frequency such that i_{Lr} lags output voltage v_{AB}. Some schematic waveforms of the system are shown in Fig. 10. For reference, the corresponding expanded waveforms around t_0 are also shown in Fig. 10(b). Fig. 11 shows the equivalent circuits of Fig. 9 in different operating status and under ZVS mode for one half cycle.

State 1: $t < t_0$

Before t_0, Q_2 and Q_4 are conducting and the corresponding equivalent circuit is shown in Fig. 11(a), It is seen that at $t = t_0$ i_{Lr} is positive and the voltages across D_2, D_4, C_2 and C_4 are zero.

State 2: $t_0 \le t < t_{01}$

During the dead time interval ($t_0 \le t < t_1$), all four active switches are turned off. At t_0, Q_2 and Q_4 are turned off and the resulting equivalent circuit is shown in Fig. 11(b). Thus, capacitors C_2 and C_4 are charged and C_1 and C_3 are discharged. Assume that $C_1 = C_2 = C_3 = C_4$, then, surge voltage $v_P(t)$ can be calculated from the equivalent circuit as shown in Fig.

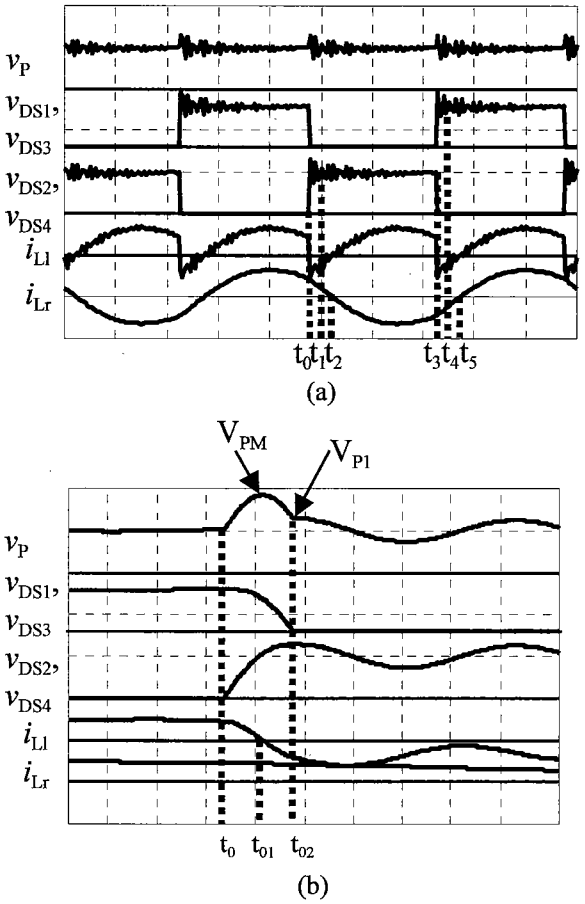


Fig. 10. Steady state waveforms (a) v_P , v_{DS1} , v_{DS3}, v_{DS2}, v_{DS4}, i_{Ll}, i_{Lr} (b) Expanded waveform around t_0 under ZVS mode

12(a) as follow:

$$V_S = L_l \frac{di}{dt'} + iR_S + v_{Ce} \tag{15}$$

$$C_e \frac{dv_{ce}}{dt'} = i \tag{16}$$

$$i(t'=0) = I_0, \quad v_{ce}(t'=0) = v_p(t'=0) = V_S$$

where $t'=t-t_0$, and

C_e = (C_1 in series with C_2)// (C_4 in series with C_3)

Hence, the resulting surge voltage

$$v_P(t') = V_S + \frac{I_0 Z_0}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_n t'} \sin(\omega_n \sqrt{1-\zeta^2}\, t' - \phi) \tag{17}$$

$$\phi = \tan^{-1}\frac{\sqrt{1-\zeta^2}}{\zeta}, \omega_n = \frac{1}{\sqrt{L_l C_e}}, Z_0 = \sqrt{\frac{L_l}{Ce}}, \xi = \frac{R_S}{2}\sqrt{\frac{Ce}{L_l}}$$

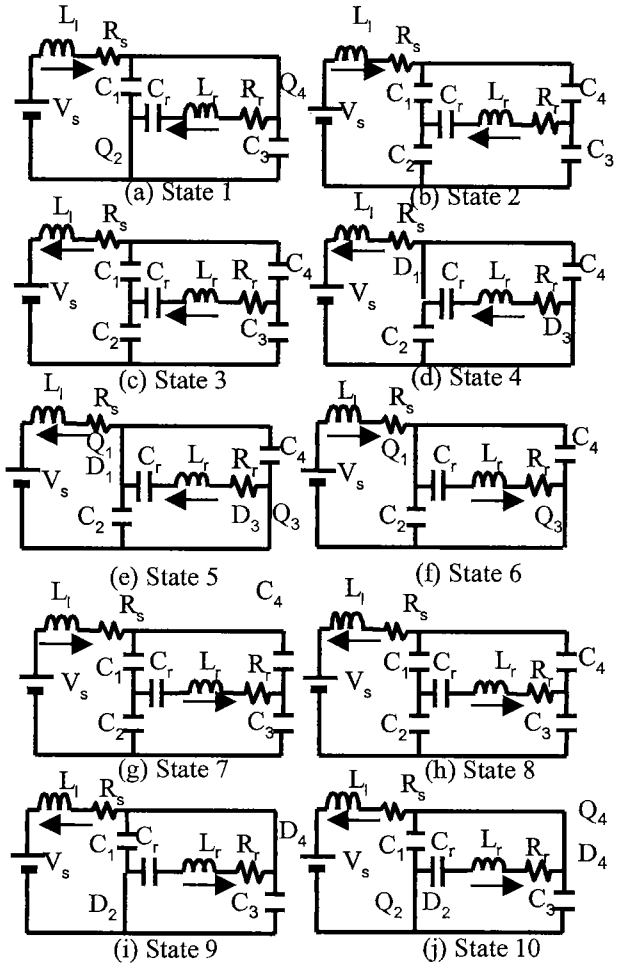


Fig. 11. Equivalent circuits in different operatin status under ZVS mode

State 3: $t_{01} \le t < t_{02}$

At t_{01}, i_{L1} decreases to zero and changes direction there after, the corresponding equivalent circuit is given as Fig. 11(c). Between t_{01} and t_{02}, surge v_P decreases gradually.

State4: $t_{02} \le t < t_1$

At t_{02}, the voltage of C_2 and C_4 are charged to V_{P1} as shown in Fig.4b, hence v_{DS2} (v_{DS4}) is equal to v_P, then D_1 and D_3 conduct. The resulting operating equivalent circuit is shown in Fig. 11(d). Thus, for $t \ge t_{02}$ $v_{DS2}(t)$ ($=v_{DS4}(t)$) will be equal to $v_P(t)$. The simplified equivalent model is shown in Fig. 12 (b) where due to the high frequency of the surge, the load current can be considered as a constant current source approximately and $C_s = C_4 + C_2$.

Thus, from Fig. 12 (b) one has

$$V_S = L_l \frac{di}{dt''} + iR_S + v_{CS} \qquad (18)$$

$$C_S \frac{dv_{CS}}{dt''} = i + I_0 \qquad (19)$$

$i(t''=0)=-I_0$, $v_{CS}(t''=0)=v_P(t''=0)=V_{P1}$

where $t''=t-t_{02}$

Hence, the resulting surge voltage

$$v_{CS}(t'') = V_S + (V_{P1} - V_S - I_0 R_S)\frac{-1}{\sqrt{1-\xi_1^2}} e^{-\xi_1 \omega_{n1} t''} \sin(\sqrt{1-\xi_1^2}\,\omega_{n1} t'' - \phi) + (V_{P1} - V_S - I_0 R_S)\frac{R_S}{Z_0}\frac{1}{\sqrt{1-\xi_1^2}} e^{-\xi_1 \omega_{n1} t''} \sin(\sqrt{1-\xi_1^2}\,\omega_{n1} t'') \qquad (20)$$

$$\omega_{n1} = \frac{1}{\sqrt{L_l C_S}}, Z_{01} = \sqrt{\frac{L_l}{C_S}}, \xi_1 = \frac{R_S}{2}\sqrt{\frac{C_S}{L_l}}$$

State 5: $t_1 \le t < t_2$

At $t = t_1$, v_{DS1} and v_{DS3} are almost equal to zero, and Q_1 and Q_3 are turned on under ZVS condition. The resulting equivalent circuit is shown in Fig. 11(e).

State 6: $t_2 \le t < t_3$

After $t = t_2$, i_{Lr} becomes negative again. The resulting equivalent circuit is shown in Fig. 11(f). Thus, the remaining half cycle will be continued in a similar manner.

From the above analysis, one can see that the surge phenomenon mainly occurs at state 2. Also, due to the soft switching function, one can see from Eq. (17), due to the small I_0, the resulting surge can be kept small. The principles of operation for the next half cycle (state 6~ state 10) resemble those of state1~ state 5. The simulation and experimental results are shown in Fig. 13.

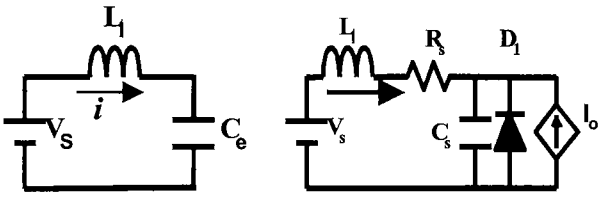


Fig. 12. (a) The equivalent circuit (ZVS mode) for calculating $v_P(t)$ in State 2
(b) The equivalent circuit (ZVS mode) for calculating $v_{DS2}(t)$ in State 4.

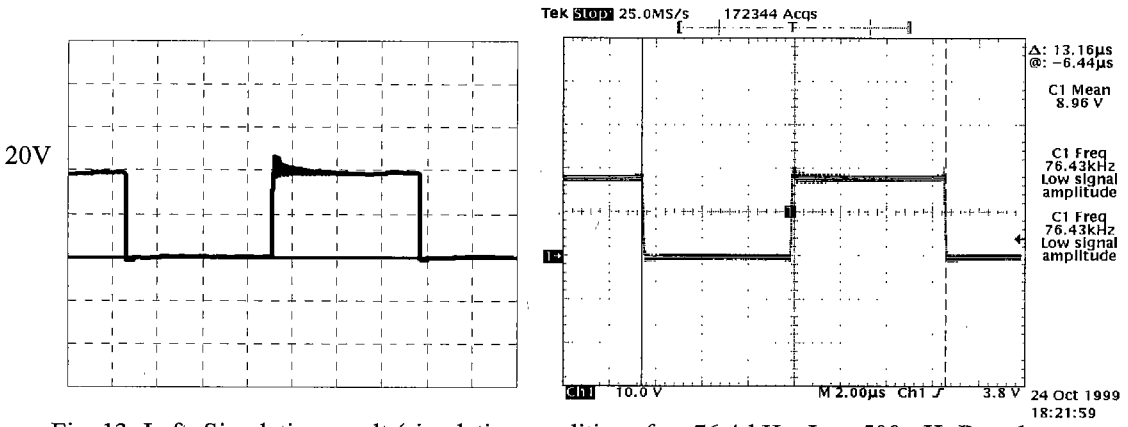


Fig. 13. Left: Simulation result (simulation condition: f_s = 76.4 kHz, L_1 = 500 nH, R_s = 1 Ω, C_1~C_4: 700 pF, L_r = 260 µH, C_r = 20 nF, R_r = 60 Ω)
Right: Experimental result (V_s = 18 V, f_s = 76.4 kHz)

5. Surge Analysis of Non-ZVS Mode

When the system operating frequency is lower than the output circuit resonant frequency, the system works in non-ZVS mode. A surge usually occurs under one of two conditions: 1. When the temperature of the work piece is higher than the Curie temperature, the inductance of the work-piece is reduced to a very small value, and thus the resonant frequency becomes very high. Operating frequency is lower than the resonant frequency, causing the inverter to work in non-ZVS mode, due to the internal maximum frequency limitation of PLL circuit. 2. In the heating process, the operating frequency does not match the resonant frequency of the output circuit in a transient condition. State analysis of the non-ZVS mode is as follows, and the timing chart is shown in Fig 14.

State 0: $t < t_{00}$

Before time t_{00}, Q_2 and Q_4 are turned off. This is known as the dead time; the current flow is shown in Fig. 15 (a).

State 1: $t_{00} \le t < t_{01}$

At instant t_{00}, Q_1 and Q_3 are turned on, causing a short circuit between v_p and negative point of V_s, i.e. v_p=0. This phenomenon is shown in the lower part of Fig. 14. The equivalent circuit and the output current flow are shown in Fig. 15 (b). Between times t_{00} and t_{01}, the current through L_1 is decreased to zero and then changes direction and increases. The current flow is shown as Fig. 15(c).

State 2: $t_{01} \le t < t_{02}$

At instant t01, i_{Ll} increases to the value of the current i_{Lr} (I_0). D_2 and D_4 begin to turn off. The recovery characteristics of the diode are such that D_2 and D_4 remain conductive *until* the integral of the reverse current reaches the stored charge of the diode. The diode becomes capacitive due to the depletion capacitance. Current flow is shown in Fig. 15 (c).

State 3 : $t_{02} \le t < t_1$

After the recovery time, D_2 and D_4 are turned off. The current path is shown in Fig. 15 (d). At this moment, the surge appears. L_1 and C_s begin to oscillate and there is a huge surge voltage in Q_2 and Q_4. The equivalent circuit is shown in Fig.16 (a). Assume that i_{Lr} is a constant current. The equivalent circuit can be simplified as in Fig.16 (b). The differential equations on the surge equivalent circuit in Fig.16 (b) are as follows.

$$V_S = L_l \frac{di_{Ll}}{dt} + i_{Ll} R_S + v_{CS}(t) \tag{19}$$

$$C_S \frac{dv_{CS}(t)}{dt} = i_{Ll} - I_0 \tag{20}$$

Assume that the body-diode recovery charge (Qr) of the power device is

$$Q_r = \frac{1}{2} I_r T_r \qquad T_r : \text{recovery time} \tag{21}$$

The initial condition of the generated surge is

$$i_{Ll}(t_{02}) = I_0 + I_r,\ v_{CS}(t_{02}) = 0$$

The surge voltage $v_{CS}(t)$ as a solution of Eqs. (19) and (20) is as follows.

$$\tau = t - t_{02}$$

$$v_{CS}(\tau) = (V_S - I_0 R_S) \times \left[1 + \frac{1}{\sqrt{1-\xi^2}} e^{-\xi\omega_n \tau} \sin(\omega_n \sqrt{1-\xi^2}\,\tau - \phi) \right] +$$

$$I_r Z_0 \frac{1}{\sqrt{1-\xi^2}} e^{-\xi\omega_n \tau} \sin \omega_n \sqrt{1-\xi^2}\,\tau \qquad (22)$$

$$\omega_n = \frac{1}{\sqrt{L_l C_S}}, Z_0 = \sqrt{\frac{L_l}{C_s}}, \xi = \frac{R_S}{2}\sqrt{\frac{C_S}{L_l}}, \phi = \tan^{-1}\frac{\sqrt{1-\xi^2}}{-\xi}$$

The criterion for surge oscillation criteria is

$$\frac{R_S^2 C_S}{4L_l} < 1 \qquad (23)$$

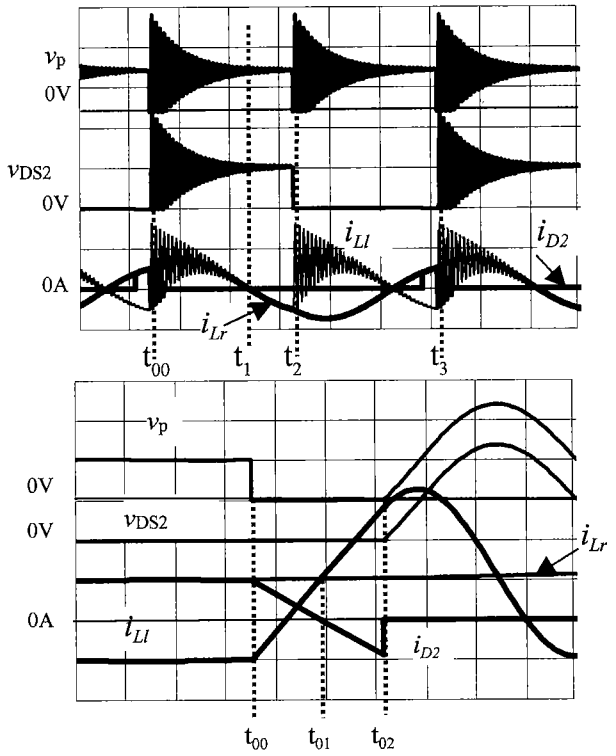


Fig. 14. Upper: timing chart of power stage in non-ZVS mode. Lower: the extension of timing chart around to (v_{DS1}~ v_{DS4} are the drain-source voltage of Q_1, Q_2, Q_3 and Q_4. v_p is the voltage on DC bus shown in Fig. 9)

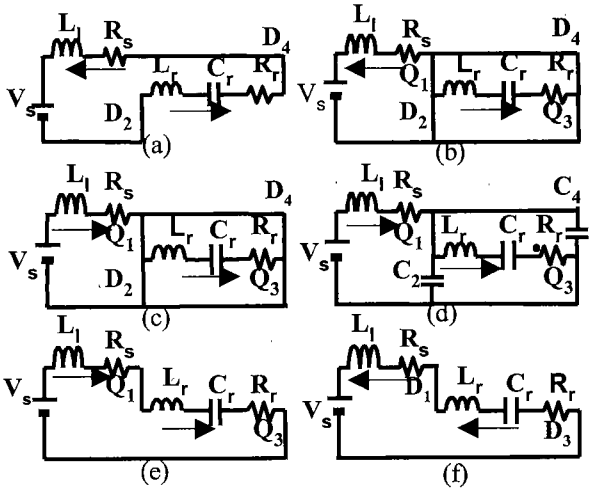


Fig.15. Circuits operation diagram in non-ZVS mode

Then, both i_{Ll} and i_{Lr} are resonant currents, which flow through L_r, C_r and R_r. The current paths are shown in Fig. 15 (e).

State 4: $t_1 \leq t < t_2$

At instant t_1, the load current changes direction, and D_1 and D_3 are turned on. The current flow path is shown in Fig. 15 (f)

State 5: $t_2 \leq t < t_3$

Q_2 and Q_4 are turned on at instant t_2, and the following resonant half cycle is understood by similar process. The experiment and simulation results are presented in Fig.17

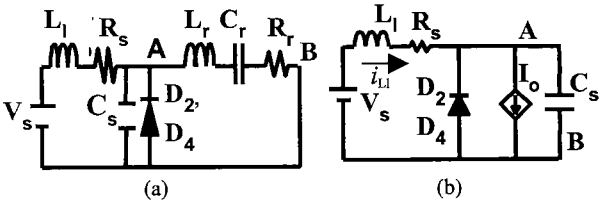


Fig.16. Surge equivalent circuit (D_2 and D_4 are recovery)

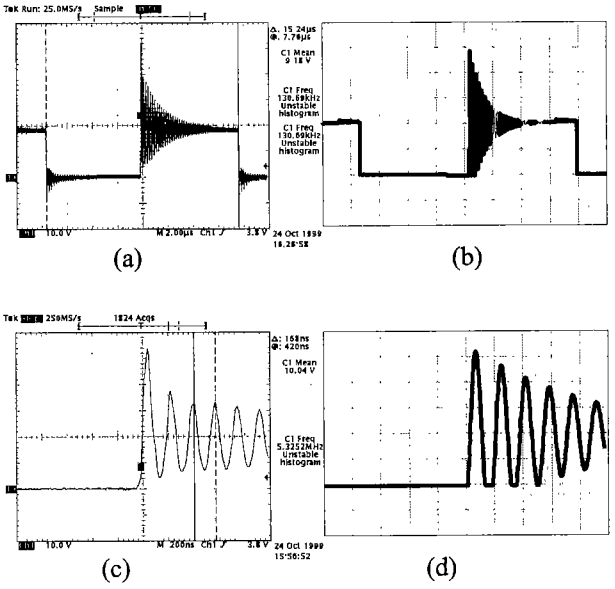


Fig.17.(a) Experimental result of waveform of V_{DS2} (V_s = 20 V, fs = 78 kHz) (20 V/DIV, 2 μs/DIV).

(b) Simulation result of waveform of V_{DS2} (simulation conditions: V_s = 20 V, L_l = 600 nH, R_s = 600 mΩ, L_r = 275 μH, C_r = 20 nF, R_r = 60 Ω, recovery energy Q_{RM}=30 nC)

(c) Extended surge waveform of Fig. 17(a)

(d) Extended surge waveform of Fig. 17(b)

6. Experimental Results

To facilitate understanding of the previous analyses and serve as verification, a prototype heating system of 2 kW rating is constructed as shown in Fig.1. Some measured parameters are listed as follows.

$L_r = 275\ \mu H$, $C_r = 20\ nF$, $R_r = 60\ \Omega$

MOSFET (IXFH26N50) of IXYS Corp.

$C_1 = C_2 = C_3 = C_4 = 700\ pF$

$Q_r = 1\ \mu C$ (when $T_j = 25\ °C$, $V_s = 100\ V$, $-di/dt = 100\ A/\mu S$, $I_F = 26\ A$). Fig. 13 and Fig.17 reveal that the surges in the power stage operating in ZVS and non-ZVS modes markedly differ from each other. In ZVS mode, the surge is very small, as shown in Fig.13. In non-ZVS mode, the surge is very large, as shown in Fig.17. Between the simulation and experimental results, one can observe that both surge frequencies agree very closely while there is a little difference in the surge amplitudes. The experimental and simulation results for the surge voltage at different switching frequencies are given in Fig.18. In this Figure, the vertical axe is the peak value of surge voltage of v_{DS2}, the horizontal axe is the output switching frequency. Again, one can see the close agreement between the simulated, calculated and measured results. Thus, the proposed simple surge model can indeed model the surge phenomenon correctly. Fig. 18 also shows that the minimum surge voltage is observed at a switching frequency of 72 kHz slightly higher than the resonant frequency of SRC. (The resonant frequency of SRC is almost 68 kHz). When the switching frequency is closer to the resonant frequency, the switching current of the power devices is lower, this phenomenon can be appreciated using the mathematical model developed in this investigation. The Phase-Locked Loop circuit is used to make the power stage operate at a frequency slightly higher than the resonant frequency of the SRC, thereby minimizing the surge voltage in the power devices. The simulation in this paper is based on the SCAT 450 software (A transient waveform simulator made by Kumamoto Institute of Technology).

In non-ZVS mode, the recovery energy of the body-diode is the main cause of large surge voltages, which can be higher than twice the source voltage. For example: IXYS MOSFET (IXFH26N50) in the case of T_j=25°C, V_r = 100 V, -di/dt=100 A/us and I_F=26 A, with recovery energy Q_{RM} is 1 μ C. The recovery energy is large enough to generate very huge surge.

In the experiment the recovery current of the body-diode is sometimes much higher than its forward current, as is shown in Fig.19. In this figure, v_p is the DC bus voltage in the power stage, which was shown in Fig.9. When Q_1 and Q_3 are turned on, v_p falls to zero. This phenomenon conforms the simulation result shown in Fig. 19. i_{Q2} is the current, which flows through power device Q_2 in the non-ZVS mode in state 1. Before t_a, the load current i_{LR} is very small and flows through the body diode (D_2) of Q_2 as a forward current. At t_a, Q_1 and Q_3 are turned on. There is a very large surge current, which goes through Q_2 as a recovery current. At t_b, a huge surge voltage is generated. It is more than twice the source voltage, Vs.

The relationship between surge voltage and power source is indicated in Fig.20. A greater load current leads to higher recovery energy in body-diode, ultimately leading to a higher surge voltage.

The reverse voltage in the body diode shown in Eq. (23) [11] determines the depletion capacitance of the diode. Fig. 20 reveals that with a source of higher voltage, C_j is smaller and causes a higher surge frequency.

$$C_j = \frac{K}{(V_0 - V_D)^m} \tag{23}$$

C_j = depletion capacitance

V_o : depletion voltage(no external voltage)

V_D : The terminal voltage on diode

K : constant decided by juction area and concentration of impurity

m : constant decided by the distribution of impurity around juction area normally is 1/3 ~ 3 or 4

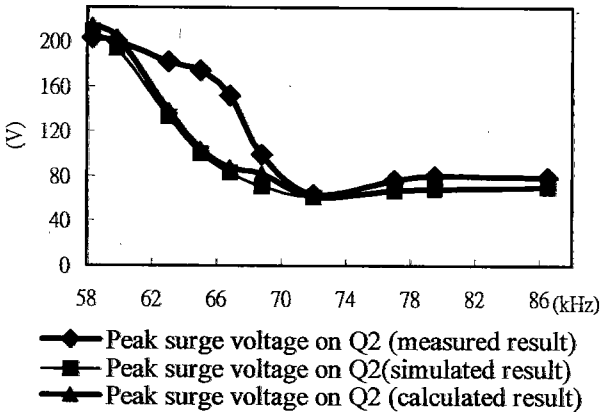


Fig. 18 Surge simulation and experimental result in the operation frequency range

(Simulation conditions: Vs = 50 V, L_l = 600 nH, R_s = 600 mΩ, L_r = 275 μH, C_r = 20 nF, R_r = 60 Ω. Experimental condition: V_s =5 0 V, f_s = 78 kHz,)

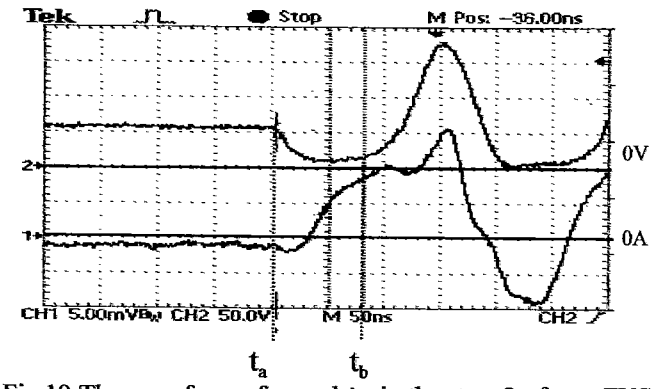


Fig.19 The waveform of v_p and i_{Q2} in the state 2 of non-ZVS mode (50 V/DIV, 1 A/DIV, 50 ns/DIV)

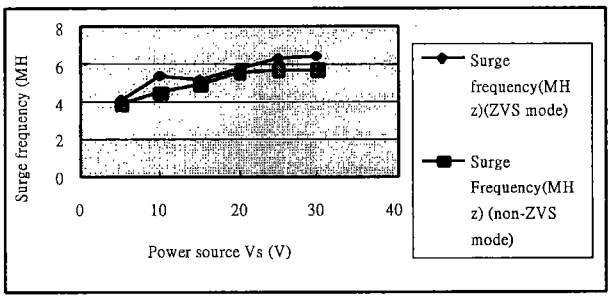


Fig.20 Surge frequencies at different power source V_s (V) (ZVS mode) (test condition: f_s = 128 kHz, non-ZVS mode fs = 79 kHz, f_r = 102 kHz, no load condition)

7. Conclusion

This investigation has demonstrated that surges are strongly related to the operation mode (ZVS mode and non-ZVS mode). This phenomenon has not been discussed in previous literature. By means of states analysis and experiment, the mechanism of surge in both ZVS mode and non-ZVS mode is made clear and surge voltage of power device is quantitatively evaluated. The mechanisms are very helpful to realize surges generated process and minimize it. Compared to surge equations, obviously the recovery energy of body-diode is the main factor to generate huge spike in the non- ZVS mode. In this mode, the surge amplitude is determined by the leakage inductance of the power line and the recovery current flowing through the body diode of the power devices (MOSFET).

The surge mechanism can be expanded to all full bridge inverters. The surge equation is useful to determine and minimize surges.

The modified PLL circuit is successful to maintain output switching frequency to be slightly higher than the resonant frequency of resonant tank, and the system can always operate in ZVS mode, ensuring that only a very small surge can be generated and power devices operate in a ZVS turn-on situation. Otherwise, the output current and the voltage are maintained almost in phase, such that output power is always maximized and circulating energy is minimized. The modified PLL control method, presented in this paper, is very useful in eliminating surges and maximizing output power. Furthermore, the simulation results and the experimental results closely correspond to each other.

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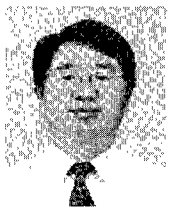

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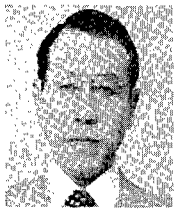

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