Paper

A Neural Network Based Behavioral Model of a Monolithic Cascode Power Switch

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Abstract

Time domain simulation is essential in computer aided design and debug of Power Integrated Circuits. Behavioral models allow to largely increase simulation speed and flexibility and are ideal for time domain simulations. A new technique is presented that allows to obtain a neural network based behavioral model of the output stage of a VIPower™ Integrated Circuit including temperature effects and employing only input/output measurements. Using the proposed approach, a temperature dependant model of a monolithic cascode switch has been developed and tested.

Key words: Power Integrated Circuit; Neural Network; Behavioral model.

1. Introduction

Power Integrated Circuits (PICs) are an emergent class of electronic devices, which integrate both power and control stages on the same silicon substrate. Major application fields of PICs are consumer electronics, lighting, automotive, TV deflection and motor control, where they allow to dramatically reduce sizes, amount of pieces, power losses and costs.

Time domain simulation is essential in PICs computer aided design and debug. Unfortunately, using conventional techniques based on physical models, the complexity of such devices and the high switching frequency featured by the addressed applications, make computer simulation expensive in terms of time and computing resources. Moreover, using conventional device models, large inaccuracy has been experienced to reproduce the device response in quasi-saturation zone [1]. Finally, standard parameter extraction techniques cannot be always applied in PICs as the device terminals are not physically or totally accessible.

Behavioral models, although less accurate than physics based models, allow to largely increase the simulation speed and flexibility, being ideal for a first evaluation of PIC main features. In this paper, by exploiting neural networks, a new approach is presented that allows to obtain a behavioral model of the output stage of a VIPower™ IC, by simply exploiting input/output measurements, including temperature effects. The developed model can be easily connected to a physic or a behavioral model of the control circuitry, allowing full modeling of a PIC.

In order to automatically extract the model from experimental data, a suitable procedure has been developed. The procedure consists in collecting a set of experimental measures and in training the Neural Network. Moreover, the proposed behavioral approach is able to forecast the key features of new devices according to a suitable database of similar devices.

2. Overview on VIPower™ Based Monolithic Cascode Devices

The power stage of a PIC is generally realized using PowerMos devices, Bipolar transistors or more efficient combined structures. A very promising configuration is the cascode connection of a low voltage Power MOS with high voltage Bipolar Transistor (BJT), since it allows to obtain a good compromise between current capability, breakdown voltage, switching frequency and efficiency.

During the on state, both the BJT and Power MOS are forward conducting, featuring a current density very close to that of a bipolar transistor of the same size [2]. The power MOS acts as a bare resistance, connected in series with the BJT.

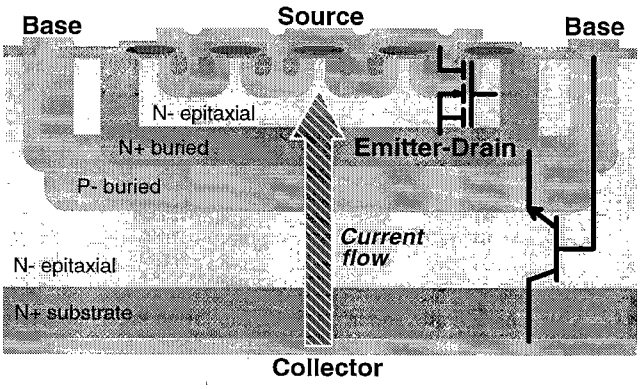


Fig. 1 – Structure of a VIPower™ based monolithic cascode power switch.

In the off state, the device behaves like a reverse biased diode, featuring high breakdown voltage equal to the collector-base junction breakdown voltage. The turn off process is very fast, since the device acts as an emitter switching structure. The Power MOSFET is firstly turned off, breaking the emitter current path.

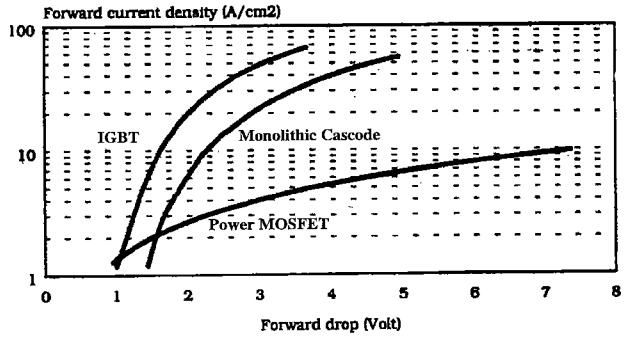


Fig. 2 - Static characteristics of 1000 V IGBT, Cascode Monolithic and Power MOSFET switches.

The collector current is then forced to flow through the base of the bipolar transistor, quickly removing the stored charge and turning off the BJT.

The Vertical Intelligent Power (VIPower™) technology allows to monolithically build on a single silicon chip a power stage with vertical current flow and low voltage circuitries. Therefore a cascode power devices are obtained by integrating both analog and digital control circuits, thus achieving a very large design flexibility.

According to Fig. 1, the basic structure of a VIPower™ based monolithic cascode power switch combines on the same silicon substrate a vertical current flow NPN transistor and a low voltage Power MOSFET, built inside the emitter of the bipolar transistor. More sophisticated structures can also be assembled where Darlington or Trilinton configurations replace the single NPN transistor, in order to reduce the base current. Since the device production process starts from an N-type substrate a complete compatibility is obtained between NPN and PIC production lines. Control and protection circuits are realized inside a diffused P-type buried layer on the same silicon substrate of the power stage. VIPower™ based monolithic cascode power switches can be designed to withstand voltages as high as 1500 V, with current capabilities ranging from .1 to 15 A. Fig. 2 shows a comparison between static characteristics of 1000 V IGBT, Cascode Monolithic and Power MOSFET switches, confirming that the performance of the Cascode Monolithic device remains in between the two standard components.

3. The Proposed Model

A neural network approach has been used to obtain a behavioral model of the cascode power switch. Such a technique allows to optimize the model accuracy, while ensuring a good simulation speed. According to the proposed approach, the switch is regarded as a black box with four external terminals: the collector and the base of the NPN transistor, the gate and the source of the Power MOSFET [3]. As shown in Fig. 3, the emitter of the NPN transistor that is coincident with the Power MOSFET drain, is regarded as an internal node and is not considered in the model. The structure of the proposed model is composed of the cascode connection of a non-linear DC model, taking into account the steady state characteristics of the device and a non-linear AC block accounting for the dynamic features.

As shown in Fig. 3, the "DC block" has three inputs and one output. The input variables are the gate-source voltage, the collector-source voltage and the base current, while the output is the collector current.

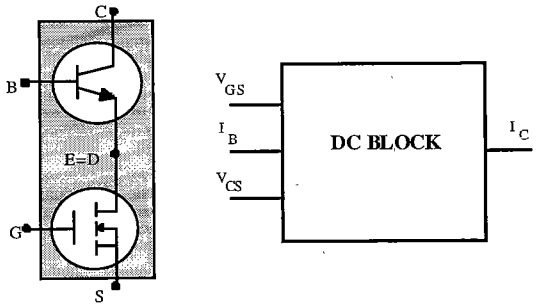


Fig. 3 – Structure of the cascode power switch and the static model.

3.1 Static model

The state of the cascode power switch is controlled by the gate-source voltage, while the collector current (I_C) depends on the collector-source voltage (V_{CS}) and the base current (I_B). Consequently, the static behavior of the device can be modelled by the following expressions:

$$I_C=0 \quad \text{if} \quad V_{GS}\le V_{TH} \text{ or } I_B\le I_{B,min} \qquad (1)$$

$$I_C=f(V_{CS},I_B) \quad \text{if} \quad V_{GS}>V_{TH} \text{ and } I_B>I_{B,min} \qquad (2)$$

Due to the non linearity of I_C, a neural network has been used to describe the previous expressions. The structure of the neural network model, as shown in Fig. 4, is composed by thirty neurones in a single hidden layer and a single neuron output layer, being w the weights and b the thresholds. Such a structure has been selected after several trials as a good compromise between precision of the simulation results and model complexity.

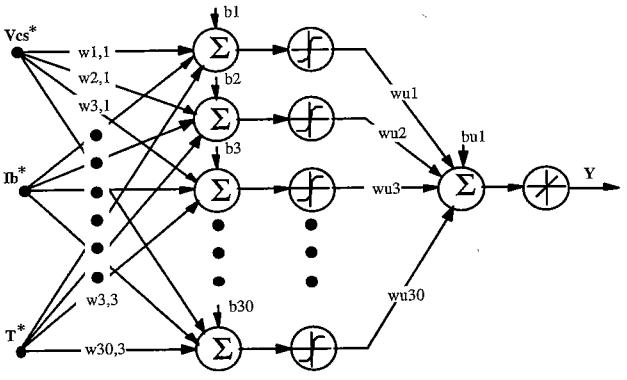


Fig. 4 – NN model structure.

The proposed neural network approach also allows to easily introduce temperature effects in the I-V characteristics of the static model. The temperature range considered is – 40 to 150 °C.

To reproduce the behavior of the real device, the neural model needs to be trained with a representative set of static I-V characteristics.

In order to obtain a suitable set of data, a curve tracer has been used to record the static response of the PIC, while a

thermo-stream has been employed to control the device temperature. The results have been processed with the Neural Network Toolbox of Matlab [4], tuning the neural model with the Temporal Backpropagation method in order to obtain suitable values of the model parameters (b_i, $wu_{i,j}$, bu_1).

3.2 Dynamic Model

In Fig. 5, the structure of the dynamic model is shown. During the on-state, the I_C current is calculated by the DC block while V_{CS} is determined by the external circuit.

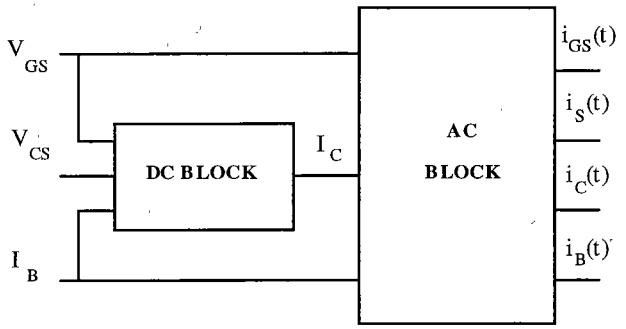


Fig. 5 – Structure of the dynamic model.

The dynamic block defines the dynamic response of the device model at turn off. As V_{GS} is driven below the threshold, the power MOS is switched off. The collector current is forced to flow trough the base of the BJT, rapidly removing the base charge and causing a fast turn off of the bipolar transistor. During the turn off, the differential equations (3), (4) and (5) with variable parameters are used to describe the model dynamic:

$$i_C(t) = \frac{I_C}{\left(1 + e^{\frac{d(t+T_f k)}{\gamma}}\right)} \qquad (3)$$

$$i_B(t) = I_B - i_C(t) \qquad (4)$$

$$i_G(t) = C_{GS} \cdot \frac{dV_{GS}}{dt} \qquad (5)$$

where d and k are suitable constant parameters.

The parameter T_f in eq. (3) allows to define the device delay time at turn off, due to the power MOS storage time, while the parameter γ corresponds to the inverse of the current slope. As the collector current waveform at turn off depends non-linearly on the collector-source voltage, as well as on the base current, the parameters T_f *and* γ have to be changed during the transient, in order to fit the real i_C behavior. In order to compute suitable values of T_f and γ, a neural network is used, owning a structure similar to that shown in Fig. 4. After some trials, a configuration using four neurons in a single hidden layer has been selected.

The neural model needs to be trained with a suitable set of measurements, reproducing the behavior of the device in the full operating range. Using the scheme described in Fig. 6, some characteristics at different collector and base currents have been recorded.

According to the test circuit performance, when the device is turned on, the inductance current grows linearly up to the desired value, then the device is switched off. At this point, the collector current goes into the base and flows through the zener diode, as the base voltage is maintained fixed at the zener voltage. During the turn off transient, the collector voltage is clamped at the value V_{clamp}, ensuring the consistency of the measurement.

Once the data have been collected and structured in a suitable form, the neural network based dynamic block is trained using the Temporal Backpropagation method. Finally, a suitable procedure automatically generates SPICE or ELDO netlists from the obtained neural network model, in order to allow the model to be connected to standard circuit models of other electronic devices.

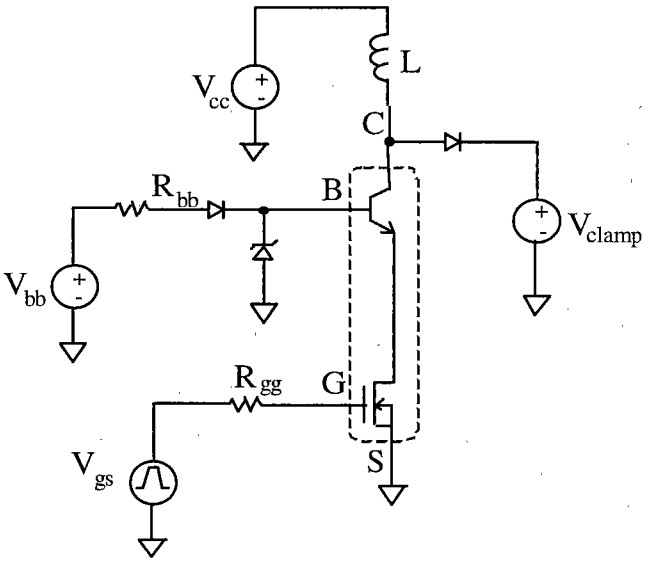
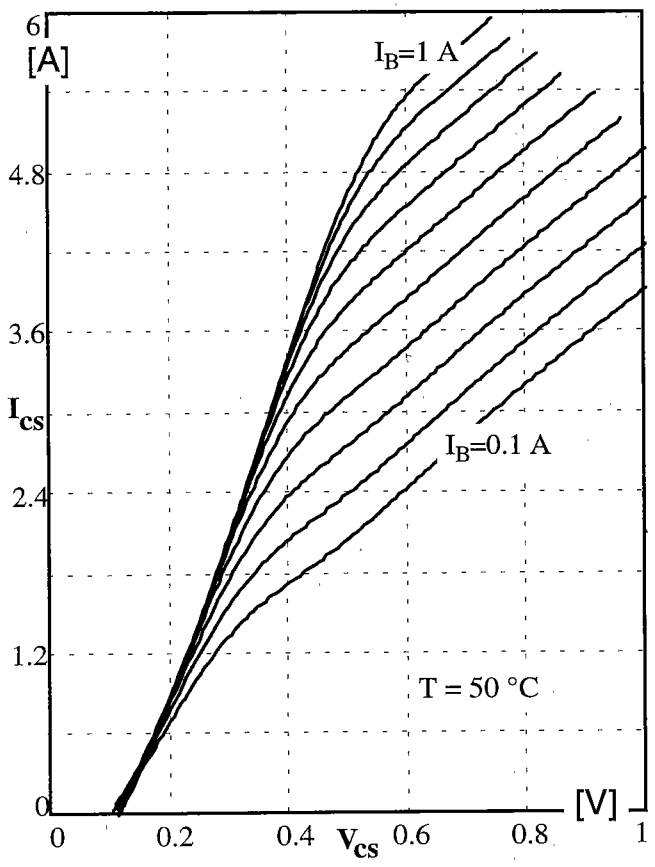


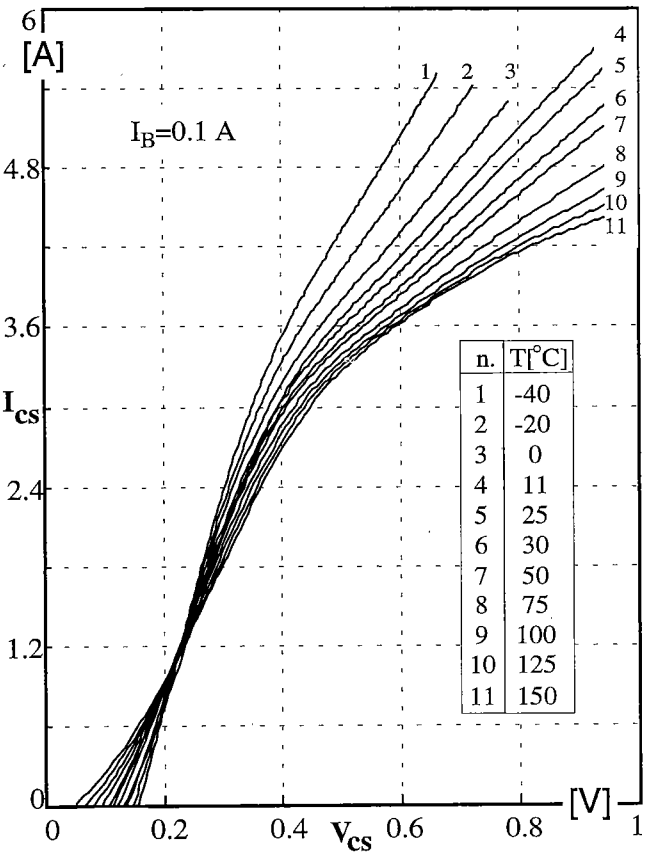
Fig. 6 – Experimental circuit for constant voltage turn-off test.

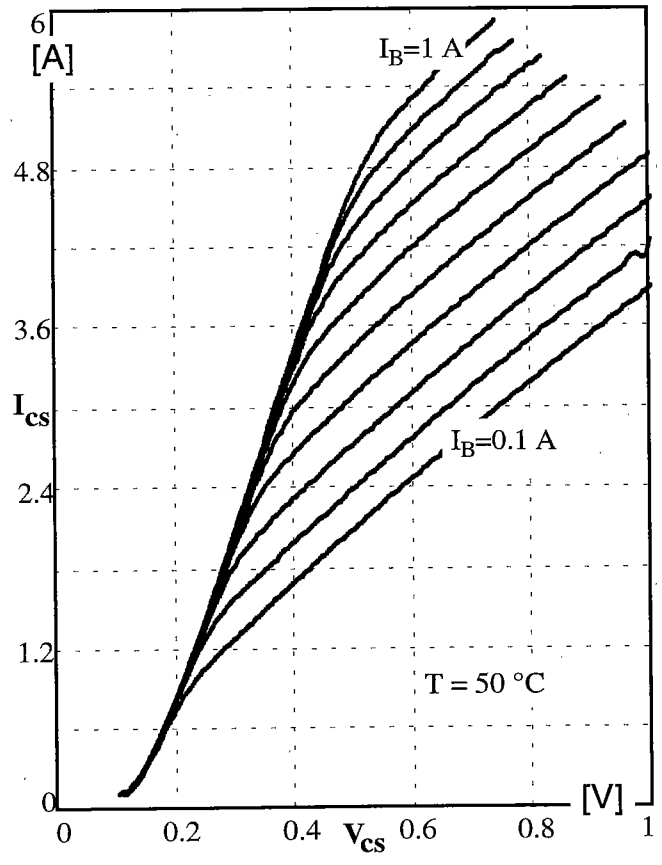
4. Model Evaluation and Validation

In order to validate the obtained model, simulation tests have been carried out and compared with experimental results. According to the test circuit shown in Fig. 6, both in experimental and simulation tests the power MOS is switched on by settling V_{GS} value up to ten volts. Fig. 7 shows the measured and simulated static I-V characteristics of a 1200 V, 6 A device. The waveforms are obtained at a 50 °C by increasing the base current from 0.1 A up to 1 A with steps of 0.1 A. Experimental and simulated curves are very close, confirming the accuracy of the static model.

In order to test the model response in the considered temperature range, a set of curves, all obtained at 0.1 mA fixed base current and different temperatures, are in Fig. 8. Each simulated curve, except those at 11 and 30 °C, has a correspondent experimental result, showing the model accuracy in reproducing the set of curves employed to train the neural network. The curves at 11 and 30 °C are predicted by the proposed model using the input/output data







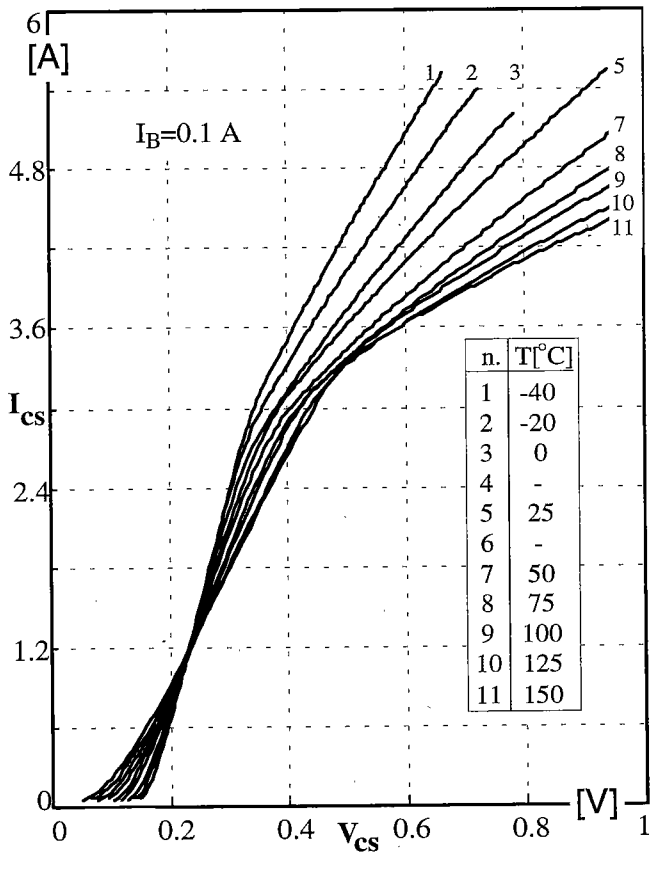


Fig. 7 - Static I-V characteristics at different I_B and constant temperature (simulated: up; measured: down).

Fig. 8 - Static I-V characteristics at constant I_B and different temperatures (simulated: up; measured: down).

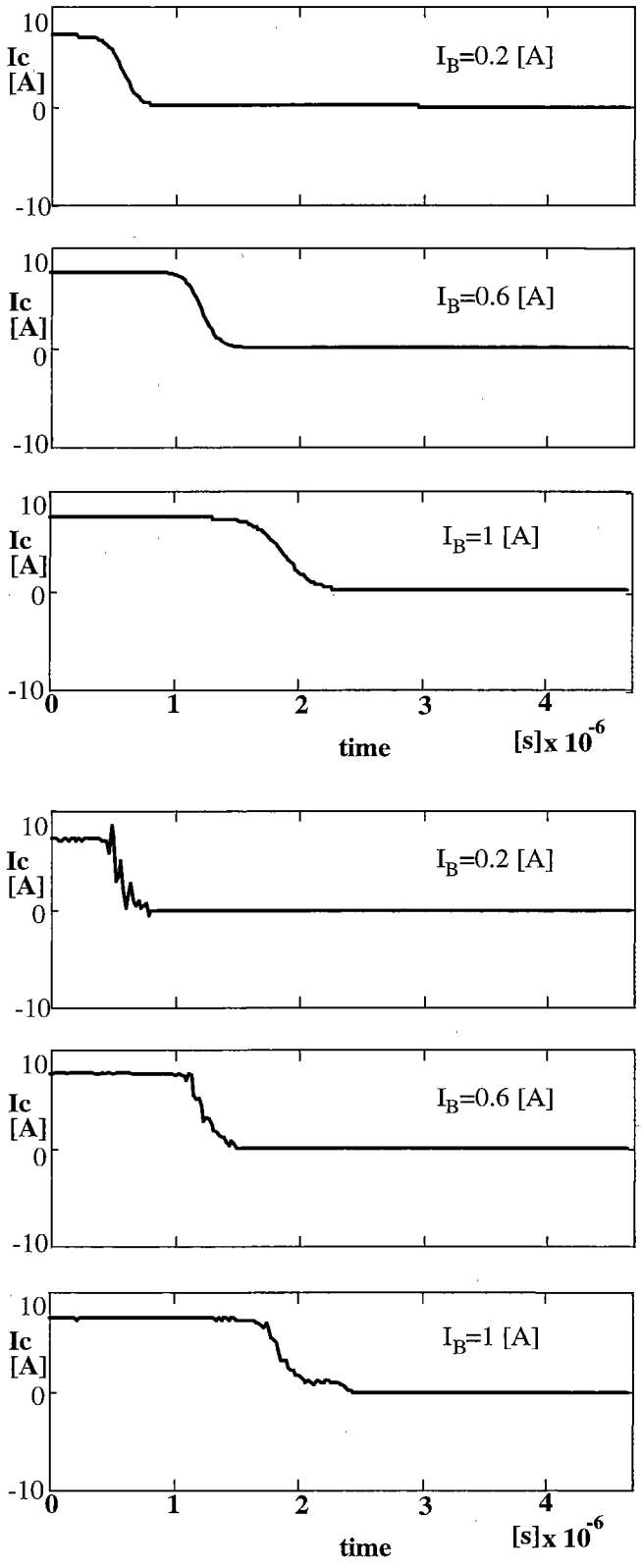


Fig. 9 – Simulated (up) and experimental (down) results of turn-off tests with different I_B.

obtained in different operating conditions and allow to evaluate the abstraction capabilities of the neural network.

In Fig. 9, a set of experimental and simulated results, dealing with the device turn off are presented, each obtained at different I_B. Using the ELDO simulation software, the model has been also employed to perform simulations of the circuit shown in Fig. 6.

Figs. 10 and 11 show simulation results dealing with switch turn off. The first time diagram describes the gate signal, while the second shows the current in the inductance and the third one the collector current. The current through the clamp diode and the collector voltage are shown, respectively, in the fourth and fifth diagrams. The last drawing shows the gate current.

By comparing the second and the third diagrams, different behaviour is observed due to the action of the clamp circuit. In fact, as the power device is turned off, the inductance current flows to the ground through the diode and the voltage source V_{clamp}. Therefore the collector voltage grows up rapidly to the value of the voltage source V_{clamp}, until the current goes to zero. As it is possible to note, the gate current remains zero except the two peaks due to the charge and discharge of the input gate capacitance of the power MOS.

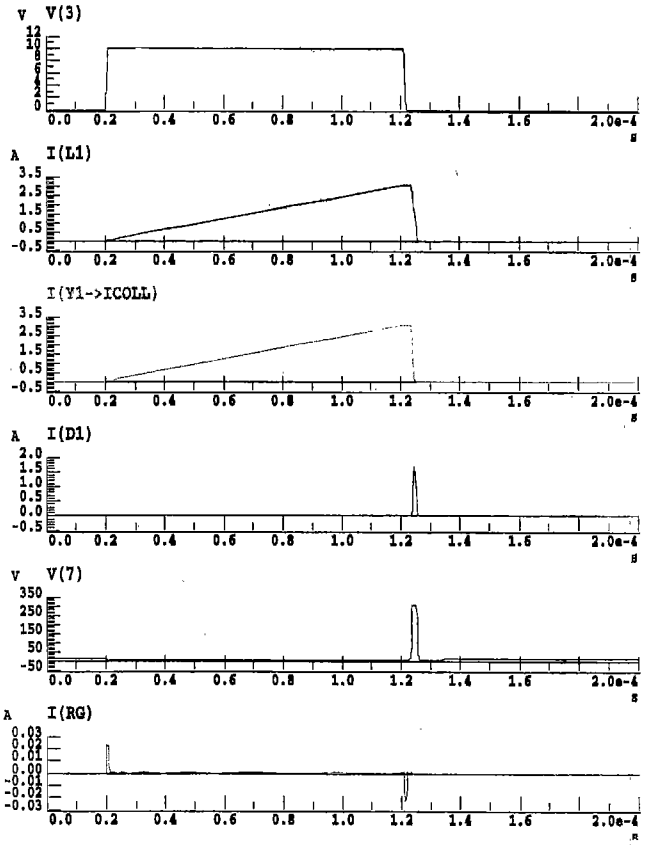


Fig. 10 – Simulation of switch turn off.

5. Conclusion

A neural approach has been presented that allows to obtain a behavioral model of a monolithic cascode switch. A suitable procedure has been developed in order to extract the model parameters from experimental tests, automatically tune the neural model and build up SPICE or ELDO netlists. Using the proposed approach, the behavioral model of a VIPower™ monolithic cascode switch has been developed, taking into account the temperature effects on static characteristics. Simulations have been carried out, showing the consistency of the proposed method.

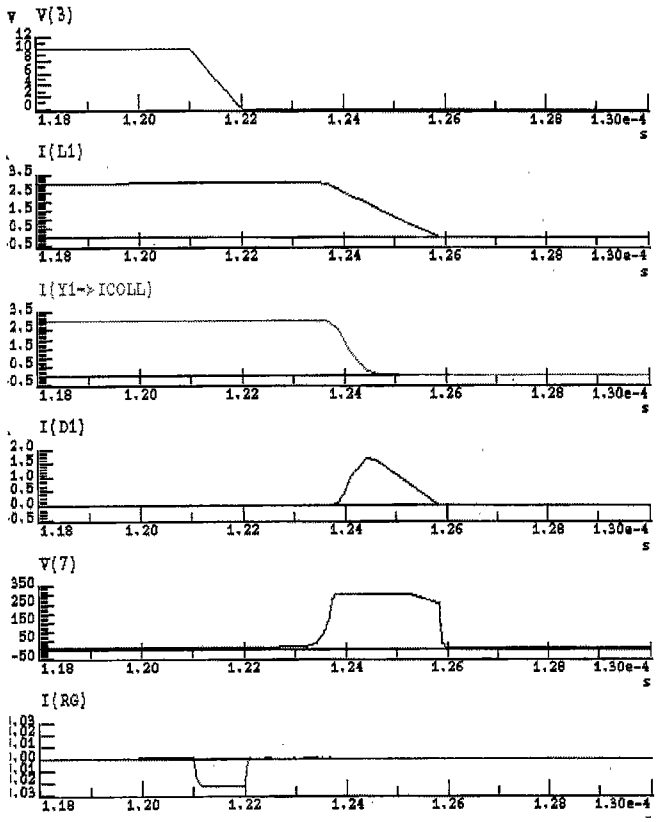


Fig. 11 – Magnification of simulation switch turn off.

The main advantage of the described approach consists in the possibility of modeling complex structures using input/output characteristics only, thus avoiding the estimation of internal parameters. Moreover, in comparison with simulations performed using standard models, behavioral modeling simulations feature shorter simulation times.

Further developments, aimed to include the temperature effect on device dynamics, are in progress.

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Mario Cacciato was born in Catania, Italy, in 1969. He received the M.S. degree with honor in 1996 in Electrical Engineering from the University of Catania, Italy, and the Ph.D. in Electronic Engineering in 2000 from the University of Reggio Calabria, Italy. Since November 2000 he joined the University of Rome "La Sapienza", Italy, as an assistant professor. He is a Member of IEEE.

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Professor Consoli is the author of more than 150 technical papers and two international patents. He has also coauthored and coeditored the book *"Modern Electric Drives"* (Amsterdam, The Netherlands: Kluwer, 2000).
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Antonio Testa was born in Catania, Italy, in 1962. He received the degree in electrical engineering in 1988 from the University of Catania, Italy. During 1989-1990, he was recipient of an SGS-Thomson Grant. From 1990 to 1998, he was an Assistant Professor of Electrical Drives and Power Electronics in the Department of Electrical, Electronic and Systems Engineering, University of Catania. He is currently a Professor of Electric Machines and Power Electronics at the University of Messina, Sant'Agata, Messina, Italy. During the 1991, he was a Visiting Researcher at the University of Wisconsin, Madison. Professor Testa is coauthor of more than 100 technical papers and two international patents. His major research interest are in the fields of sensorless control of electrical drives, advanced digital control systems, power converters, power devices and electromagnetic compatibility.
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