Paper

A Control IC for an Optocoupler-less DC-DC Converter with a Current Mirror Detection Circuit

Non-member Masamitsu Inaba (Hitachi Research Laboratory, Hitachi, Ltd.)
Non-member Masahiro Iwamura (Hitachi Research Laboratory, Hitachi, Ltd.)
Member Noboru Akiyama (Hitachi Research Laboratory, Hitachi, Ltd.)
Non-member Michiaki Ono (Telecommunication Systems Division, Hitachi, Ltd.)
Non-member Nobuaki Tajimi (Telecommunication Systems Division, Hitachi, Ltd.)
Non-member Keiichi Sukegawa (Hitachi Haramachi Electronics Co., Ltd.)

A control IC has been developed that can provide a small flyback DC-DC converter without an optocoupler. This IC has new detection and control circuits using current mirrors and level-shift circuit technology. It reduces the mounting area of the DC-DC converter by 30%, and the DC-DC converter exhibits constant-voltage characteristics and conversion efficiency comparable to those of conventional converters.

Keywords : Control IC, DC-DC Converter

1. Introduction

Smaller power supplies are needed for electronic equipment, such as mobile PCs (personal computers) and telecommunication devices. Consequently, power-supply components like transformers, inductors, rectifiers, and main switches are being miniaturized or integrated into control circuits[1],[2].

As shown in Fig. 1, a conventional flyback DC-DC converter consists of a transformer, a filter, a control circuit, a main switch, a detection circuit, and an optocoupler. The input voltage, V_i, and the output voltage, V_o, are isolated by the optocoupler. The isolation voltage of the optocoupler between the input side and the output side is several thousand volts. However the integration of the optocoupler into the monolithic IC is difficult.

Figure 2 shows applications of DC-DC converter used for telecommunications. In this case, the loads are telephones, facsimiles and personal computers. In addition, high impedance resistors connect a terminal, V_+ or V_-, with ground. The reason is that if the terminal V_+ or V_- is completely floating, the output voltage V_+ or V_- increases up to dangerous high voltage. In such applications, high impedance between the terminal V_+ or V_- and ground is required, but high voltage isolation is not necessary.

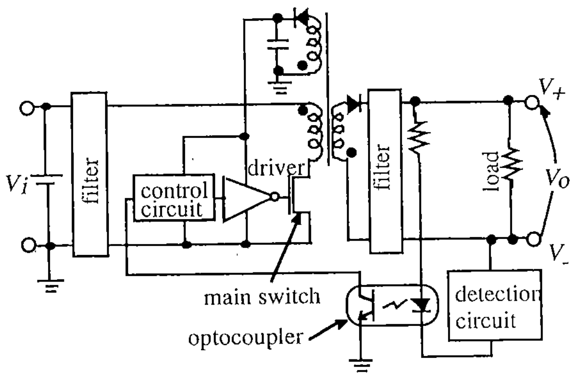


Fig. 1. Schematic diagram of a conventional flyback DC-DC converter.

Therefore, the optocoupler can be replaced by a high impedance current mirror circuit. It is noted that this technology can not be used in the purpose of the high voltage (>300 V) isolation. This paper describes a control IC for a flyback DC-DC converter that uses current mirrors and a level-shift circuit instead of an optocoupler.

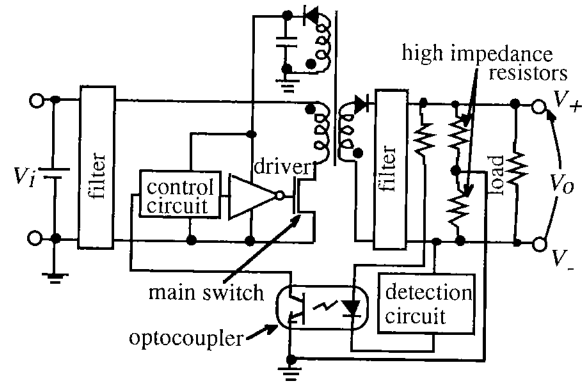


Fig. 2. An application of DC-DC converter for telecommunication

2. Design Considerations

2.1 New Flyback DC-DC Converter

As shown in Fig. 3, in our flyback DC-DC converter, the optocoupler is replaced with a detection circuit and a level-shift circuit using current mirror technology. The output voltage and current of the converter are detected by current mirror circuits, and the standard level of output voltage V_o is changed to that of input voltage V_i by the level-shift circuit. An auxiliary power supply consists of a basic step-down switching regulator with a series reactor. The current mirror detection circuit, the level-shift circuit, the control circuit, the auxiliary power supply and the driver circuit are integrated on one chip, thereby reducing the mounting area of the converter.

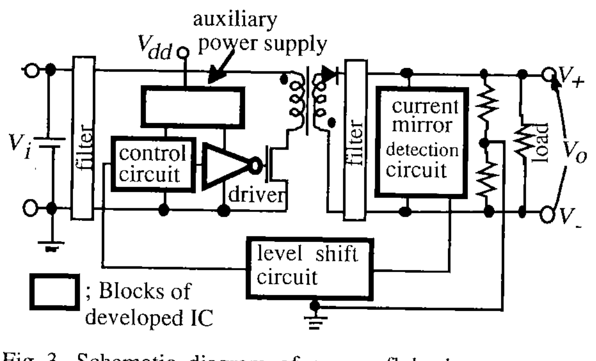


Fig. 3. Schematic diagram of a new flyback DC-DC converter.

2.2 New Detection Circuit

The principle of the detection circuit is illustrated in Fig. 4. The output voltage of the auxiliary power supply, V_{dd}, is generated on the input side of the DC-DC converter. The voltage of V_{dd} is higher than that of the output terminal V_- because of operating current mirror circuits CM_1 and CM_2. Current mirror circuit CM_1 consists of Q_1 and Q_2, and CM_2 consists of Q_3 and Q_4. The output voltage of the DC-DC converter, which appears on a floating level, is transformed into current I_{a1}. Current I_{a1} flows to resistor R through CM_1 and CM_2. If h_{FE} of Q_1, Q_2, Q_3 and Q_4 are very large, the collector current of Q_2 and Q_4, I_{a2} and I_{a3}, are almost same as I_{a1}. Consequently, detection voltage V_d ($= I_{a1} \times R$) appears on ground level. Detection voltage V_d passes into the DC-DC control circuit. We estimate the output impedance of current mirror circuit. In the current mirror circuit, the following basic equations are obtained:

$$I_{a1} - 2\,I_b = I_{a2} \quad \cdots\cdots\cdots (1)$$

$$I_b = I_{a2} \cdot h_{FE}' \quad \cdots\cdots\cdots (2)$$

$$h_{FE}' = h_{FE} \cdot (1 + V_{CE}/V_a) \cdots (3)$$

where I_b is the base current of Q_2, V_{CE} is the voltage between the collector and emitter of Q_2 and V_a is the Early voltage of Q_2. In the output characteristics of bipolar transistors, the I-V lines intersect the negative axis at approximately one point, which is called Early voltage[3]. From (1) and (2), we obtain the following equation:

$$I_{a1} = I_{a2} \cdot (1 + 2/h_{FE}') \cdots (4)$$

By using (3), we have the following equation:

$$I_{a1} = \left(1 + \frac{2}{h_{FE} \cdot (1 + V_{CE}/V_a)}\right) I_{a2} \cdots (5)$$

When we differentiate the equation (5), we have the following equation:

$$dV_{CE}/dI_{a2} = \frac{h_{FE} \cdot V_a}{2\,I_{a2}} \left(1 + \frac{2}{h_{FE} \cdot (1 + V_{CE}/V_a)}\right) \times (1 + V_{CE}/V_a)^2 \cdots (6)$$

Considering that Early voltage V_a is sufficiently large, (6) can be approximated as follows:

$$dV_{CE}/dI_{a2} \fallingdotseq h_{FE} \times V_a / I_{a2} \cdots (7)$$

Therefore, the output impedance of CM_1 is $h_{FE} \times V_a / I_{a2}$. If $h_{FE} = 100$, $V_a = 200$ V, and $I_c = 20\ \mu$A, the output impedance is 1 GΩ. This is enough impedance. Because, in the use of telecommunications, the output impedance is almost 200 kΩ-300 kΩ.

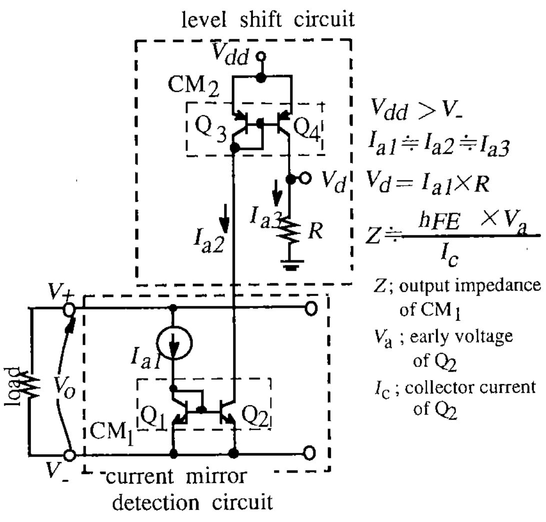


Fig. 4. Principle of a new detection circuit.

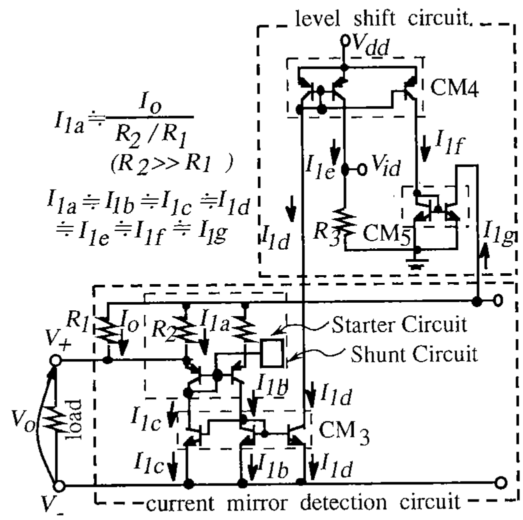


Fig. 5. Scheme of a output current detection circuit.

The output-current detection circuit of the DC-DC converter is illustrated in Fig. 5. The output current I_O of the converter is shunted by resistors R_1 and R_2. Current I_{1a} , which flows to resistor R_2 , is the source current of a shunt circuit. The shunt circuit consists of a basic current mirror circuit and a starter circuit. The current mirror circuit of the shunt circuit starts operating when the starter circuit puts a very small current into the current mirror circuit. The shunt circuit outputs current I_{1b}. The I_{1b} is almost the same as the I_{1a} because the shunt circuit is composed of current mirror circuit. The I_{1b} is the source current of current mirror circuit CM_3 .The CM_3 outputs current I_{1c} and current I_{1d} . The I_{1c} and *the* I_{1d} are almost the same as the I_{1b} . The I_{1d} is the source current of current mirror circuit CM_4. The CM_4 outputs current I_{1e} and current I_{1f} . The I_{1e} and *the* I_{1f} are almost the same as the I_{1d} .Then current I_{1a} is transformed into detection voltage V_{id} ($V_{id} \fallingdotseq I_{1e} \times R_3 \fallingdotseq I_{1a} \times R_3$). The I_{1f} is the source current of current mirror circuit CM_5 , and the CM_5 outputs Current I_{1g} . The CM_5 is the current-compensation circuit for canceling I_{1d} from the CM_3 to V_- ($I_{1g} \fallingdotseq I_{1f} \fallingdotseq I_{1d}$). To operate the CM_3 , the CM_4 , and the CM_5 , an auxiliary power supply V_{dd} is required.

The output-voltage detection circuit of the DC-DC converter is illustrated in Fig. 6. Current I_{2a} flows to resistor R_4 with output voltage V_o . The principle of the output-voltage detection circuit is the same as that of the output-current detection circuit. I_{2a} also flows to resistor R_5 through CM_6 and CM_7 . I_{2a} is transformed into detection voltage V_{do} . Current mirror circuit CM_8 is a current-compensation circuit like CM_5 .

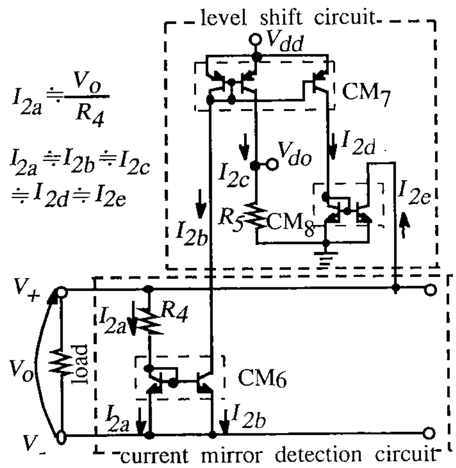


Fig. 6. Scheme of a output voltage detection circuit.

2.3 Control Circuit

The control circuit (Fig. 7) is controlled using pulse-width modulation (PWM). It consists of an error amplifier (EA), an comparator (Comp), an oscillator (OSC), etc. The standard voltage of the EA is generated by a band-gap reference circuit. There are two control modes: constant current and constant voltage. Depending on the load of the DC-DC converter, a selector chooses either detection output voltage V_{id} or V_{do} . The feedback loop gain of the control circuit is regulated by discrete capacitor C_F and resistor R_F . When an over-current flows through main switch M, the over-current protection circuit (OCP) stops the driver circuit of main switch M.

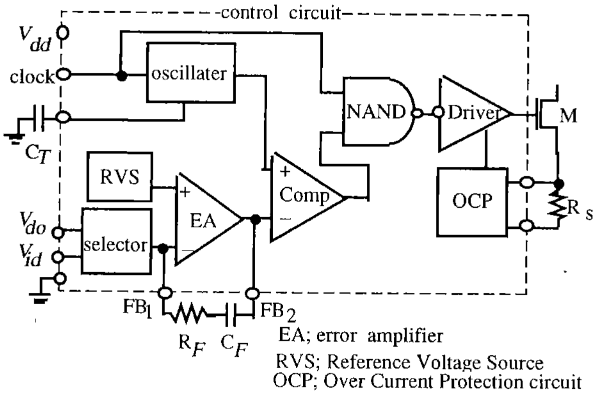


Fig.7. Block diagram of PWM control circuit

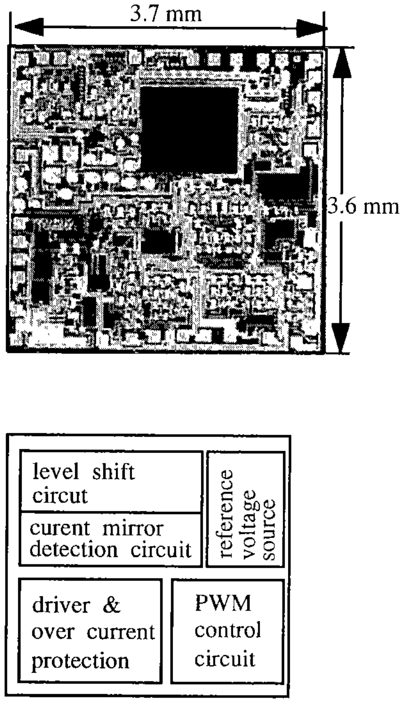


Fig.9. Photograph of the control IC for DC-DC converter.

Figure 8 shows a time chart of the control circuit. Each waveforms represent the output of the clock, EA, OSC, Comp, and NAND. The clock frequency is about 300 kHz. When the output electric power of the DC-DC converter increases, the output voltage of the EA rises and the pulse width of the NAND output widens. The clock is also entered into the NAND input. For this reason, even when the EA output is raised too much by a rapid load change, the duty cycle of the NAND output does not become more than 50%. Consequently, an over-shoot of the output of the DC-DC converter can be prevented.

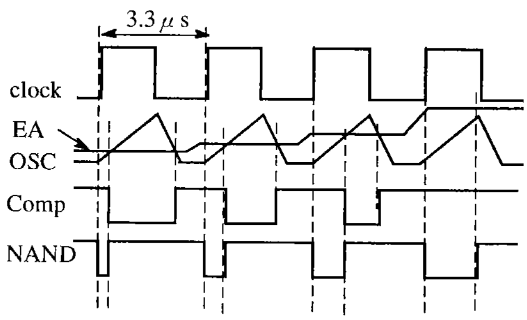


Fig.8. Time chart of PWM control circuit

3. Experimental Results

Figure 9 shows a photograph of the control IC we developed for a DC-DC converter. The chip size is 3.7 mm × 3.6 mm. It was manufactured using high-voltage bipolar process technology. Bipolar transistors with a breakdown voltage of 15-70 V were used for the PWM control circuit. Bipolar transistors with a breakdown voltage of 150-320 V were used for the current mirror detection circuit and the level shift-circuit. This IC is protected by some varisutors, so the breakdown voltage of 150-320 V is enough.

Figure 10 shows the output characteristics of a conventional flyback DC-DC converter and a developed one at room temperature. The input voltage was 40-60 V. The developed converter's characteristics was generally as good as the conventional one's. However, the accuracy of developed detection circuit was a little worse than that of conventional one. Because there was parasitic capacitor of 200 - 300pF in the bipolar transistors of developed detection circuit. As the ripple of DC-DC converter brought an inductive current into the parasitic capacitor, the inductive current caused an error of detection. As a results, the developed converter's characteristics of constant voltage was a little worse than that of conventional ones. In case of reducing the ripple, the accuracy of the detection improved better. Though the parasitic capacitor influenced the stabilization of feedback loop gain and transient characteristics, they could be adjusted by capacitor C_F and resistor R_F which were illustrated in Figure 7. The constant voltage accuracy of the developed converter was ±5% in an output characteristic, and the constant current accuracy was the same.

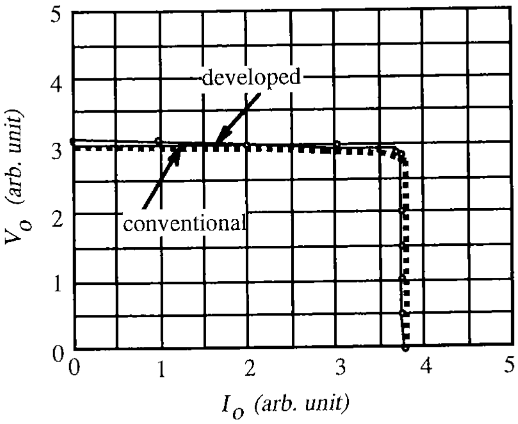


Fig.10. Output characteristics of flyback DC-DC converter using developed control IC.

Figure 11 shows the power loss and efficiency of the flyback DC-DC converter. The horizontal axis expresses the output power (P_o), and the vertical axis expresses the power loss (P_L) and efficiency (η). The solid circles show the power loss of the new flyback DC-DC converter and the solid squares show its efficiency. The P_L was 0.41 W at the $P_o = 2.25$ W. The η is $100 \times P_o/P_i = 100 \times P_o/(P_o+P_L)$, where P_i is an input power of DC-DC converter. So the η is about 85 % at $P_o = 2.25$ W. The open circle shows the power loss of a conventional flyback DC-DC converter, and the open square shows its efficiency. The difference between the conventional converter's power loss and the new one's is caused by the detection circuit. The new detection circuits can be integrated because it is designed to be a simple circuit of current mirror. As a result, the power loss of new detection circuit was smaller than that of conventional one. The efficiency of the new DC-DC converter was a little higher than that of the conventional one.

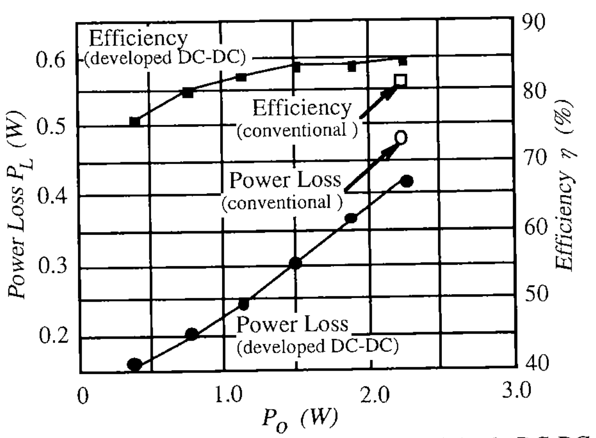


Fig.11. Power loss and efficiency of flyback DC-DC converter using developed control IC.

Figure 12 shows the mounting area of both flyback DC-DC converters. The mounting area of the new one is 30 % less than that of the conventional one. The 20 % in the total reduction ratio (30 %) is caused by the replacement of the optocoupler in the detection circuit. The rest 10 % is caused by the main circuit. In the conventional DC-DC converter, the auxiliary power supply is necessary for the detection circuit. On the other hand, the auxiliary power supply was integrated into the developed IC. So the mounting area of the main circuit was reduced 10 %. The part for the detection circuit was reduced considerably.

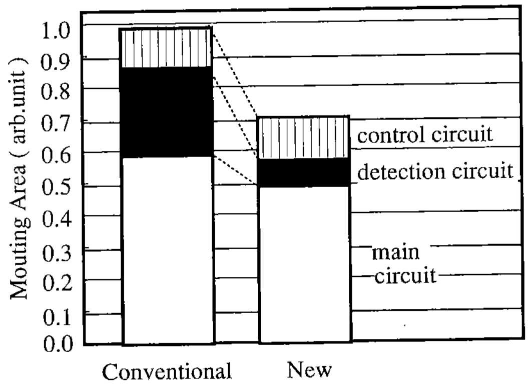


Fig.12. Mounting area of flyback DC-DC converter.

4. Conclusion

A control IC for optocoupler-less flyback DC-DC converters has been developed. It uses a new detection circuit and a level-shift circuit using a current mirror circuit. A DC-DC converter using this control IC generally exhibited good constant-voltage characteristics. The efficiency of this converter was a little higher than that of a conventional one. The mounting area was reduced 30 %.

5. Acknowledgments

We thank Mr.I.Oohinata,Mr. N. Yukawa,Mr. J. Kitano, Mr. K. Arita and Mr.M. Miura for their continuing encouragement and support.

(Manuscript received Jan. 10, 2001, revised Jun. 14, 2001)

References

[1] T.Serada, K.Tsukamoto, and T.Yachi, "Small, Highly Efficient Battery Input Type 1W Class DC-DC Converters", Proceedings of IPEC-Yokohama'95, pp.417-421,1995.

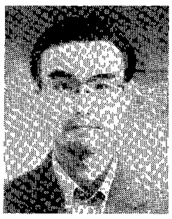
[2] R.Sodhi, S.Brown Sr., and D.Kinzer, "Integrated Design Environment for DC-DC Converter FET Optimization", Proceedings of ISPSD'99, pp.241-244,1999.

[3] Adolph Blicher, "Field-Effect and Bipolar Power Transistor Physics," ACADEMIC PRESS, pp.115-116,1981.

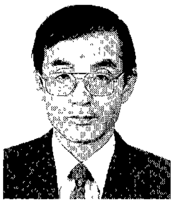
[4] W.Tang, Y.Jiang, G.C.Hua, and F.C.Lee, "Power Factor Correction with Flyback Converter Employing Charge Control," Proceedings of IEEE Applied Power Electronics Conf., pp.293-298,1993.

[5] R.Erickson, M.Madigan, and S.Singer, "Design of a Simple High-Power-Factor Rectifier Based on the Flyback Converter," Proceedings of IEEE Applied Power Electronics Conf., pp.792-801,1990.

[6] M.Jordan, "Load Share Simplifies Parallel Power Supply Design," Proceedings of Power Conversion Conf., Sept.1991.



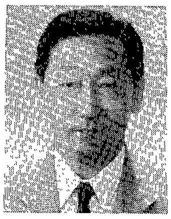
Masamitsu Inaba (Non-Member) was born in Iwate, Japan, on May 18, 1967. He graduated from Tohoku University, Miyagi, Japan, in 1992. He joined Hitachi Research Laboratory, Hitachi, Ltd., Ibaraki, Japan in 1992. He has been engaged in research and development of high-voltage ICs.



Masahiro Iwamura (Non-member) was born in Saga, Japan, on June 28, 1942. In 1961 he jointed Hitachi Research Laboratory, Hitachi, Ltd., Hitachi, Japan. From 1961 to 1981 he was engaged in research and development of computer control system, mini-computer and high precision color CRT display apparatus. From 1982 to 1994 he was engaged in research and development of BiCMOS circuit for CISC,RISC microprocessor and fast SRAMs. Since 1994 He has been engaged research and development of power IC circuit. He performed architecture and logic design of famous CRT display controller (6845CRTC). He has been awarded 50 U.S. patents in CRT display apparatus, microprocessor, CMOS/BiCMOS circuits and fast SRAM.

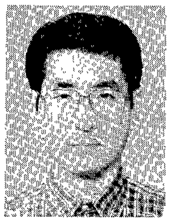
He is now a senior researcher at Hitachi research laboratory Hitachi, Ltd. His active research interests include mixed IC of high voltage and low voltage integrated circuits.

Mr. Iwamura is a member of the Institute of Electronics, Information and Communication engineers of Japan.



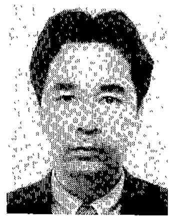
Noboru Akiyama (Member) was born in Tokyo, Japan, on March 24, 1956. He received the B.S. and M.S. degrees in electronic engineering from Waseda University, Tokyo, Japan, in 1978 and 1980, respectively. He joined Hitachi Research Laboratory, Hitachi, Ltd., Ibaraki, Japan, in 1980, where engaged in research and development of BiCMOS memories and high-voltage ICs. His current research interest is in the development of system LSI technology.

Mr. Akiyama is a member of the Institute of the Electrical Engineers of Japan, the Institute of the Electronics, Information and communication engineers of Japan, and the IEEE Solid-State Circuits Society .



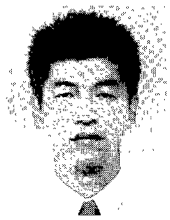
Michiaki Ono (Non-member) was born in Hokkaido, Japan in 1965. He graduated from Hokkaido Institute of Technology in 1988. In 1988 he joined Telecommunication Systems Division, Hitachi, Ltd., Yokohama, Japan. He has been engaged in the development of Subscriber Line System.

Mr.Ono is a member of the Institute of Electronics, Information and Communication Engineers of Japan.



Nobuaki Tajimi (Non-member) was born in Gifu, Japan in 1960. He graduated from Gifu Technical College in 1981. In 1981 he joined Hitachi Ltd. Telecommunication Systems Division, Yokohama, Japan. He has been engaged in the development of Subscriber Line System.

Mr.Tajimi is a member of the Institute of Electronics, Information and Communication Engineers of Japan.



Keiichi Sukegawa (Non-Member) was born in Ibaraki, Japan, on November 19, 1971. He joined Hitachi Haramachi Electronics Co., Ltd., Ibaraki, Japan, in 1990. He has been engaged in research and development of BiCMOS memories and high-voltage ICs. His current research interest is in 16-Bit Microcontroller.