FPGA design of a digital circuit for estimating chaotic characteristics from approximated nonlinear functions

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In this paper, an FPGA circuit for estimating chaotic characteristics of unknown nonlinear systems is proposed. From particular solutions corresponding to chaotic signals of the unknown system, the proposed circuit approximates nonlinear functions. The approximation of these nonlinear functions are performed by using supervised learning. From the approximated functions, chaotic characteristics of the unknown system are estimated. An understanding of the behavior of unknown nonlinear system will be provided by utilizing the estimated chaotic characteristics. The proposed circuit is implemented onto an FPGA by using Verilog-HDL. This implementation confirmed that the proposed circuit can achieve high-speed operation and low-cost development.

Keywords: chaos circuits, FPGA implementation, fuzzy systems, supervised learning

1. Introduction

Chaos is the most frequently encountered phenomenon in the study of nonlinear dynamical systems such as biological neural networks [1], power systems [2],[3], and so on. For example, in medical field, chaos can be observed in brain pulse, R-R interval in electrocardiogram (ECG), and so on. In the studies of these nonlinear dynamical systems which exhibit chaotic behavior, it is important to understand their mechanism. The studies of nonlinear dynamical systems have been carried out by utilizing computer simulations. However, they require long computational time [2]-[6]. For this reason, a chaos circuit is one of the most efficient tools for experimental observation of chaos. In previous studies, many physical, biological and chemical systems have been studied by means of large ensembles of interacting analog chaos circuits [7]-[9]. Among those, Pivka has modeled traveling waves by using resistor-coupled Chua's circuits [9]. However, it is difficult for these method to make rigorous models of unknown nonlinear systems, because they cannot accurately represent the nonlinear functions. Therefore, we attempt to make the models by applying particular solutions which correspond to chaotic signals generated from the unknown nonlinear systems. The modeling of unknown nonlinear system is achieved by approximating the nonlinear function from chaotic signals. This approximation enables us to estimate chaotic characteristics of the unknown nonlinear systems. In other words, the system which can approximate nonlinear functions behaves as a chaos generator for estimating chaotic characteristics of unknown nonlinear systems.

Being distinct from above mentioned purpose, the hardware implementation of these nonlinear systems is important. The conventional software implementation on a digital computer requires an expensive high-speed microprocessor and large-capacity memories only for generating chaotic signals. The electronic circuits can be implemented by using a digital technique or an analog technique. Among others, the digital hardware implementation by using FPGA's (Field Programmable Gate Array) [10] excels in hardware cost and exact reproducibility of signals. Furthermore, FPGA-implementation can afford high-speed parallel data bus operations easily.

In this paper, an FPGA circuit for estimating chaotic characteristics of unknown nonlinear systems is proposed. From particular solutions corresponding to chaotic signals of the unknown system, the proposed circuit approximates nonlinear functions. The approximation of these nonlinear functions are performed by using supervised learning. From the approximated functions, chaotic characteristics of the unknown system are estimated. An understanding of the behavior of unknown nonlinear system will be provided by utilizing the estimated chaotic characteristics. The functional verification and logic synthesis for the proposed circuit are performed by using Verilog-HDL (Hardware Description Language) [10].

2. Architecture

Figure 1 shows a general architecture of the proposed circuit. The circuit consists of N nonlinear function blocks. † The nonlinear function block is built with a

[†]The number of nonlinear function block, N, is defined by users.

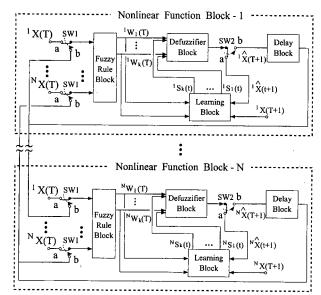


Fig.1 General architecture of the proposed circuit.

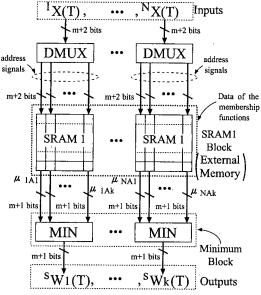


Fig.2 Architecture of the fuzzy rule block.

fuzzy based circuit consisting of a fuzzy rule block, a defuzzifier block, a learning block, and a delay block. During the learning process, the switches SW1's and SW2's are connected to a's. In this process, the nonlinear functions $F_s(\cdot)$ $(s=1,\ldots,N)$ are approximated from A/D converted chaotic signals, ${}^1x(T),\cdots,{}^Nx(T)$. After the learning process, these switches are connected to b's. Then, the nonlinear function blocks generate digital signals corresponding to estimated chaotic signals.

The detail of respective building blocks will be described in the following subsections.

2.1 Fuzzy Rule Block The inference rules FR_i 's [11] used in the nonlinear function block are given by the form:

$$FR_i$$
: If x is A_i then y is B_i , $(i = 1, 2, ..., k)$ (1)

where x is an input variable, y is an output variable, A_i 's are fuzzy set defined by the membership functions [11], and B_i is a fuzzy singleton, $1/S_i(t)$ [12].

In the fuzzy rule block, the matching degrees $W_i(T)$'s are determined by

$$^{s}W_{i}(T) = \min (\mu_{1}A_{i}(^{1}x(T)), \dots, \mu_{N}A_{i}(^{N}x(T))), (2)$$

$$(i = 1, 2, ..., k)$$
 $(s = 1, 2, ..., N)$

where T denotes the count of input signals, ${}^1x(T)$, ${}^2x(T)$, ..., and ${}^Nx(T)$ are the T-th A/D converted chaotic signals, sA_i denotes the fuzzy label [13] for the input sx in the i-th fuzzy rule, k is the number of inference rules, s is the number of nonlinear function blocks, and $\mu_{{}^1A_i}$, $\mu_{{}^2A_i}$, ..., and $\mu_{{}^NA_i}$ are the membership functions. The domain and range of $\mu_{{}^sA_i}$'s and ${}^sx(T)$'s are the sets of integers on the interval $[-2^m, 2^m]$, where m is an integer parameter. Hence, in point of accuracy, a design which has a larger number of m is preferable. The value of m is determined by considering the tradeoff between the circuit size and the accuracy.

Figure 2 shows the architecture of fuzzy rule block. In Fig.2, k fuzzy membership functions for $2^{m+1}-1$ different input values are stored in the s-th SRAM1. The size of each SRAM1 is $(m+1)(2^{m+1}-1)$ bits. As address signals for SRAM1, the demultiplexer DMUX provides $^sx(T)$'s. For the inputs, the SRAM1 block selects the values of membership functions with no sign-bit from the results-table stored in the respective SRAM1's. The minimum operation in Eq.(2) is realized in the minimum block composed of N-input/1-output MIN circuits. By selecting the minimum value of membership functions, the minimum block outputs the matching degrees $^sW_i(T)$'s.

2.2 **Defuzzifier Block** In the defuzzifier block, the output fuzzy set, ${}^sW_1(T)$ / ${}^sS_1(t) + \ldots + {}^sW_k(T)$ / ${}^sS_k(t)$, is defuzzified by the center of area (COA) method [12], where ${}^sS_i(t)$ is a singleton's element, / is Zadeh's separator, and + is a union operation. The output of defuzzifier block, ${}^s\hat{x}(t+1)$, corresponds to an estimated (T+1)-th chaotic signal. The defuzzified output ${}^s\hat{x}(t+1)$ is given by

$${}^{s}\hat{x}(t+1) = \frac{\sum_{i=1}^{k} {}^{s}S_{i}(t) {}^{s}W_{i}(T)}{\sum_{i=1}^{k} {}^{s}W_{i}(T)}, \quad (s=1,2,\ldots,N)$$

$$\stackrel{\triangle}{=} \frac{\sum_{i=1}^{k} {}^{s}S_{i}(t) {}^{s}W_{i}(T)}{2^{m}}, \quad \cdots \qquad (3)$$

where t denotes the count of learning cycle. To simplify the circuit, the membership functions are chosen such that the summation of matching degree $\sum_{i=1}^k {}^sW_i(T)$ in Eq.(3) becomes the constant value 2^m .

Figure 3 shows the circuit architecture of defuzzifier block. The scaled multiplication result ${}^sS_i(t){}^sW_i(T)/2^m$ is provided from the results-table stored in the SRAM2. The bit-length of scaled multiplication result is m+1 bits. And the size of SRAM2 used in the multiplier block is $(m+1)2^{2m}$ bits. † The

The dimension of proposed circuit is determined by the parameter N.

[†]The size of SRAM2 can be reduced to as low as $(m+1)2^m$ by

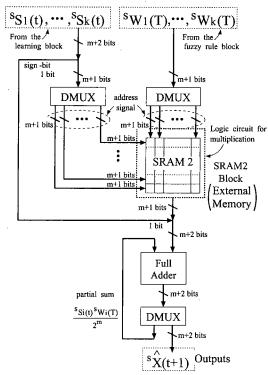


Fig.3 Architecture of the defuzzifier block.

adder block calculates the partial sum of summation in Eq.(3). After k-1 of additions, the adder block outputs the defuzzified result of Eq.(3).

2.3 Learning Block The singleton's elements ${}^sS_i(t)$'s are determined in the learning block. In the learning process, (T+1)-th chaotic signals ${}^sx(T+1)$'s are given as supervisor signals. To simplify the circuit design and to avoid the long computational time, the learning dynamics is given by

$${}^{s}S_{i}(t+1) = {}^{s}S_{i}(t) + \frac{({}^{s}x(T+1) - {}^{s}\hat{x}(t+1)) {}^{s}W_{i}(T)}{2^{m}} \cdot (4)$$

Figure 4 shows the circuit architecture of learning block. In this figure, the hatched functional blocks are shared by the learning block and the defuzzifier block since these blocks do not work simultaneously. The subtraction in Eq.(4) is realized by the subtractor. The multiplication and the partial sum of summation in Eq.(4) is realized by the same manner as the defuzzifier block. The learning process terminates when

$$| {}^{s}S_{i}(t+1) - {}^{s}S_{i}(t)| < \epsilon, \cdots (5)$$

where ϵ is a parameter.

2.4 **Delay Block** After the learning process, the nonlinear function blocks operate as a digital circuit generating the estimated chaotic signals. From Eq.(3), the dynamics of the nonlinear function blocks is given by

adopting quarter-square principle. However, this SRAM size reduction can be achieved at the cost of additional hardware (1 full-adder and 2 subtractors) and m+1 clock delay.

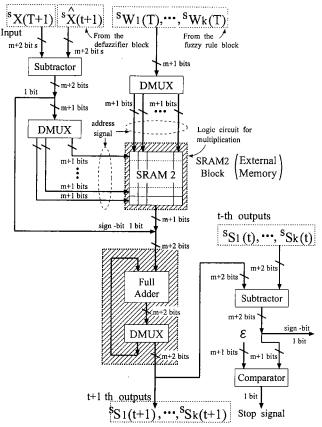


Fig.4 Architecture of the learning block.

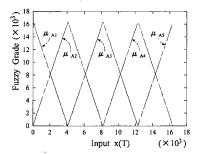


Fig.5 Membership functions for a tent map.

$${}^{s}\hat{x}(T+1) = \hat{F}_{s}({}^{1}\hat{x}(T), \dots, {}^{N}\hat{x}(T))$$

$$= \frac{\sum_{i=1}^{k} {}^{s}\hat{S}_{i} {}^{s}W_{i}(T)}{2^{m}}, \dots \dots \dots (6)$$

where ${}^s\hat{S}_i$'s are the final values of singletons. In Eq.(6), ${}^sW_i(T)$'s are determined by Eq.(2). The delay block produces a unit delay in Eq.(6) and feeds the delayed output.

3. Simulation

3.1 Numerical Simulation Firstly, to confirm the validity of algorithm, numerical simulations were performed. In the numerical simulations, two types of nonlinear functions were assumed as unknown systems. The nonlinear functions were approximated from the signals which are generated by the following maps:

$$^{1}x(T+1) = F_{1}(^{1}x(T)),$$

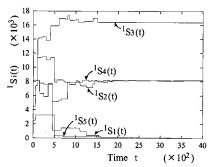


Fig.6 Convergence behaviors of the singletons for a tent map.

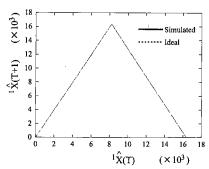


Fig.7 Approximated nonlinear function for a tent map.

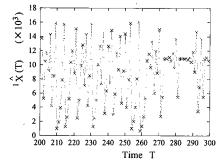


Fig.8 Estimated chaotic signal for a tent map.

$$= 2^{m} - 2|^{1}x(T) - 2^{m-1}|, \quad \cdots \qquad (7)$$

Hénon map:

$${}^{1}x(T+1) = F_{1}({}^{1}x(T), {}^{2}x(T)),$$

$$= 2^{m} + {}^{2}x(T) - (7 \times 2^{m}/5)^{1}x(T)/2^{m},$$

$${}^{2}x(T+1) = F_{2}({}^{1}x(T), {}^{2}x(T)),$$

$$= (3 \times 2^{m}/10) {}^{1}x(T)/2^{m}. \dots (8)$$

In Eqs.(7) and (8), the parameter m was set to 14. These maps are the most famous nonlinear maps for which a rigorous proof of chaotic behavior has been accomplished. In numerical simulations for the tent map, the following membership functions were used. †

• Membership functions for the tent map:

$$\mu_{Ai}(x) = 2^m - 4|x - 2^{m-2}(i-1)|, \quad (i = 1, ..., 5). \quad (9)$$

Figure 5 shows the triangular membership functions obtained from Eq.(9) †† . In case of the tent map, the

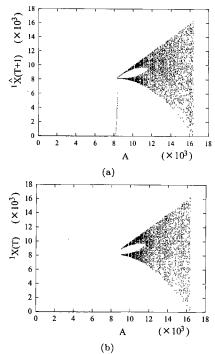


Fig. 9 Bifurcation diagram for a tent map. (a) Bifurcation diagram obtained from the approximated nonlinear function. (b) *Ideal* bifurcation diagram.

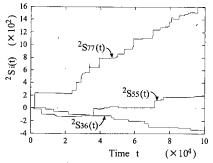


Fig.10 Convergence behaviors of the singletons for a Hénon map.

number of singletons is set to 5. Figure 6 shows the convergence behavior of singletons for the tent map. In the numerical simulations for the tent map, the count of learning cycle t was set to satisfy T = 50t. In Fig.6, the values of singleton's elements converge to their final values after 4000 learning cycles. This result means that the proposed circuit requires only 80 input data to approximate the nonlinear function of tent map. Figure 7 shows the examples of approximated nonlinear functions obtained by using the final values of singletons of Fig.6. The error of the approximated function is less than 2%. Figure 8 shows an example of the estimated chaotic signal obtained from Fig.8. In this figure, the initial value $\hat{x}(0)$ is set to 10. Although the estimated chaotic signal in Fig.8 is different from the signal generated from Eq.(8), it has similar characteristics. By multiplying the approximated nonlinear function by the parameter $A/2^m$ $(A \in [0, ..., 2^m])$, the bifurcation dia-

linear dynamical system is unknown. By applying the triangular membership functions, the nonlinear functions are approximated as piecewise-linear functions.

[†]Of course, the shape and the number of membership functions can be defined by users since the membership functions are stored in SPAM1

 $^{^{\}dagger\dagger}$ In the numerical simulations, the triangular membership functions were used. Actually, the shape of nonlinear functions of non-

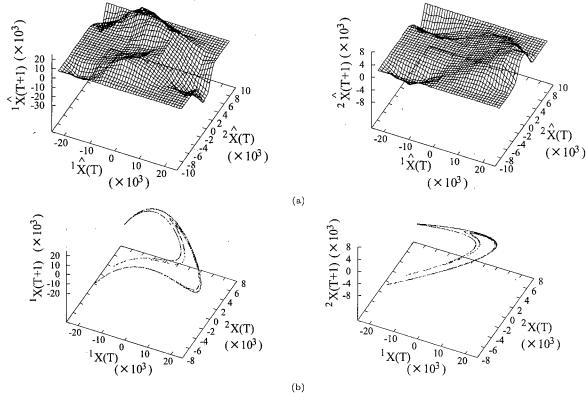


Fig.11 Nonlinear functions for a Hénon map. (a) Approximated nonlinear functions. (b) Ideal nonlinear functions obtained from Eq.(8).

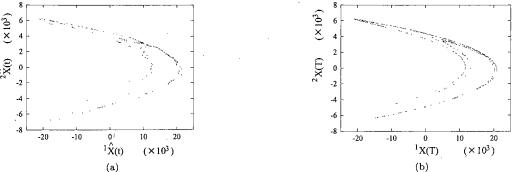


Fig.12 Strange attractor of a Hénon map. (a) Generated from the approximated nonlinear function. (b) Generated from the ideal nonlinear function

gram of the approximated tent map is obtained. Figure 9 (a) shows the bifurcation diagram obtained from the approximated tent map. Figure 9 (b) shows the *ideal* bifurcation diagram obtained by

$${}^{1}x(T+1) = AF_{1}({}^{1}x(T))/2^{m},$$

= $A\{2^{m} - 2|{}^{1}x(T) - 2^{m-1}|\}/2^{m}.$

Because of rounding error, these bifurcation diagrams make a difference in the bifurcation modes. Since the approximated nonlinear function for Fig.9 (a) satisfies $F_1(0) > 0$, the bifurcation diagram of Fig.9 (a) has a lot of difference in the period-1 orbit.

In the numerical simulations for the Hénon map, the following membership functions were used.

• Membership functions for a Hénon map:

$$\mu_{Ai}(^{1}x) = 2^{m} - 3|^{1}x + (2^{m}/3)(i - 11/2)|,$$

$$\mu_{Ai}(^{2}x) = 2^{m} - 9|^{2}x + (2^{m}/9)(i - 11/2)|,$$

$$(i = 1, \dots, 10). \dots (10)$$

In case of the Hénon map, the number of singletons, k, was set to $200~(=10\times10\times2)$. Figure 10 shows the convergence behavior of singletons for the Hénon map. In this figure, the convergence behavior of 36th, 54th, and 77th singletons for $\hat{F}_2(^1\hat{x}(T), ^2\hat{x}(T))$ are shown as examples. In the numerical simulations for the Hénon map, the count of learning cycle t was also set to satisfy T=50t. In Figs.10, the values of singleton's elements converge to their final values after 100000 learning cycles. This result means that the proposed circuit requires 2000 input data to approximate the nonlinear function of Hénon map. Figure 11 shows the examples of the approximated nonlinear functions obtained by using the final values of singletons of Fig.10. Figure 12 shows an example of the strange attractor obtained

Table 1 Results of the circuit design.

Device	Occupied CLBs	810/1024	(79%)
	Bonded I/O pins	63/192	(33%)
XC4025ePG223	Highest clock		
	frequency	19.4	(MHz)
	Critical path delay	52	(ns)

by Fig.11 (a). In Fig.12, the initial values, ${}^{1}\hat{x}(0)$ and ${}^{2}\hat{x}(0)$, are set to 10. The errors of the approximated functions are less than 4%. Here, the error Er of the approximated function is defined by

$$Er \triangleq \frac{\sqrt{\sum_{T=10000}^{20000} \{\hat{\mathbf{F}}_s(\ ^1x(T),\ ^2x(T)) - \ ^1x(T+1)\}^2}}{10000 \times \ 2^{14}} \times 100 \ (\%). \ (11)$$

Figs.8 and 12 show that the proposed circuit can generate the estimated chaotic signals from the approximated nonlinear functions.

4. Circuit Design Using Verilog-HDL

According to the architecture shown in Sect.2, the one-dimensional portion of the proposed circuit was implemented onto an FPGA using Verilog-HDL. In this design, the number of inference rules k was set to 5 and the parameter m was set to 14. And SRAM1 and SRAM2, which are used as external memory, are separated from the chip. The circuit was synthesized by the logic synthesizer with Xilinx FPGA logic unit library XC4000e which targets FPGA XC4025ePG223 [10]. The results of FPGA design are summarized in Table 1, where CLB and I/O stand for Configurable Logic Block and Input/Qutput, respectively [10]. †

5. Discussion

5.1 Error of approximated functions

The precision of approximated nonlinear function depends on the number of singletons as well as the parameter ϵ . Figure 13 shows the approximated nonlinear function of a logistic map for the number of singletons k=(5,7,9,11,13, and 15). The signals to approximate the nonlinear function are generated by

$$^{1}x(T+1) = 4^{1}x(T)(2^{m} - {}^{1}x(T)). \cdots (12)$$

Figure 14 shows the error of the approximated nonlinear function in Fig.13. Figs.13 and 14 show that the error of approximated nonlinear function can be reduced by increasing the number of singletons.

5.2 Convergence conditions of singletons

From Eqs.(3) and (4), the dynamics of learning can be expressed by

$${}^{s}\vec{S}(t+1) = (I - {}^{s}W_{B} {}^{s}W_{A}/2^{2m}) {}^{s}\vec{S}(t) + {}^{s}x(T+1) {}^{s}W_{B}/2^{m}, \cdots (13)$$

where

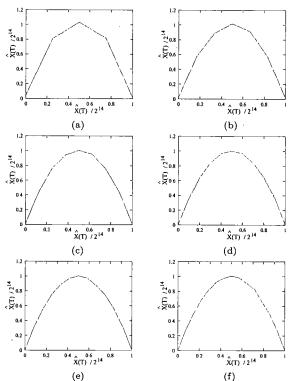


Fig.13 Approximated nonlinear function. (a) k = 5. (b) k = 7. (c) k = 9. (d) k = 11. (e) k = 13. (f) k = 15.

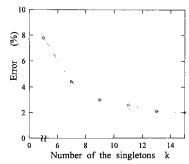


Fig.14 Error of the nonlinear function shown in Fig.13.

$${}^{s}W_{A} = \begin{bmatrix} {}^{s}W_{1}(T) & {}^{s}W_{2}(T) & \cdots & {}^{s}W_{k}(T) \\ {}^{s}W_{1}(T) & {}^{s}W_{2}(T) & \cdots & {}^{s}W_{k}(T) \\ \vdots & \vdots & \ddots & \vdots \\ {}^{s}W_{1}(T) & {}^{s}W_{2}(T) & \cdots & {}^{s}W_{k}(T) \end{bmatrix},$$

$${}^{s}W_{B} = \begin{bmatrix} {}^{s}W_{1}(T) & 0 & \cdots & 0 \\ 0 & {}^{s}W_{2}(T) & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & {}^{s}W_{k}(T) \end{bmatrix},$$

and

$$I = \begin{bmatrix} 1 & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & 1 \end{bmatrix}, \quad {}^s\vec{S}(t) = \begin{bmatrix} {}^sS_1(t) \\ {}^sS_2(t) \\ \vdots \\ {}^sS_k(t) \end{bmatrix}.$$

If k = N and sW_A and sW_B are regular matrices, Eq.(13) can be expressed by

[†]From Fig.1, high-dimensional circuits can be realized by arraying the one-dimensional portions of proposed circuit. By using the array structure, FPGA-implemented circuit can afford high-speed parallel operation.

$$\stackrel{s\vec{S}(t+1) - {}^{s}x(T+1)W_{A}^{-1}2^{m}}{= (I - {}^{s}W_{B} {}^{s}W_{A}/2^{2m})}
\stackrel{(s\vec{S}(t) - {}^{s}x(T+1)W_{A}^{-1}2^{m}), \cdots (14)}{}$$

Since Eq.(14) can be expressed by

$$\begin{split} {}^s\vec{S}(t) - {}^sx(T+1)W_A^{-1}2^m \\ &= (I - {}^sW_B \ {}^sW_A/2^{2m}) \\ & ({}^s\vec{S}(t-1) - {}^sx(T+1)W_A^{-1}2^m), \\ {}^s\vec{S}(t-1) - {}^sx(T+1)W_A^{-1}2^m \\ &= (I - {}^sW_B \ {}^sW_A/2^{2m}) \\ & ({}^s\vec{S}(t-2) - {}^sx(T+1)W_A^{-1}2^m), \end{split}$$

the following equation can be obtained:

$$\stackrel{s}{S}(t) - {}^{s}x(T+1)W_{A}^{-1}2^{m}
= (I - {}^{s}W_{B} {}^{s}W_{A}/2^{2m})^{t}
({}^{s}\vec{S}(0) - {}^{s}x(T+1)W_{A}^{-1}2^{m}). \dots (15)$$

From Eq.(15), it is the convergence condition of learning process that all the absolute values of eigen values of $I-{}^sW_B{}^sW_A/2^{2m}$ are less than 1. The membership functions must satisfy above condition to converge the singletons.

5.3 Comparison with conventional methods

Table 2 shows the comparison with conventional methods. In Table 2, the modeling using mutually-coupled chaos circuits is one of the most famous methods to investigate nonlinear dynamical systems [7]-[9]. In point of accuracy, the estimation employing digital computers is the most excellent method. However, the proposed hardware systems provide low-cost and high-speed realization. The circuit can be used as an experimental tool to understand the mechanism of unknown nonlinear systems, a classification tool exploiting the form of attractors, and so on.

6. Conclusion

In this paper, an FPGA circuit for estimating chaotic characteristics from approximated nonlinear functions has been proposed. The simulation results showed that the proposed circuit can approximate the nonlinear functions and can generate digital signals which correspond to estimated chaotic signals. Both the numerical simulations of algorithm and the synthesis of FPGA circuit showed that the one-dimensional portion of proposed circuit can be implemented onto a single FPGA except for SRAM.

The theoretical analysis for the definition of shape of

Table2 Comparison.

	Proposed circuit	Mutually-coupled chaos circuits	Software based method
Accuracy of			
Estimation	\triangle^{\dagger}	× ^{††}	0
Calculation			
speed	0		×
Hardware			
cost	0		×
Hardware			
size	0		· ×

 \dagger The accuracy of approximated nonlinear functions depends on the number of singletons, k.

†† The mutually-coupled chaos circuits are difficult to approximate the nonlinear functions since the target is unknown.

membership function is left to the future study.

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