Paper

Reduction of the surge voltage at motors fed from IGBT inverter drives by PWM correction.

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In this paper, we analyze the conditions when surge voltage peaks higher than 2 p.u (2 times the inverter DC link voltage) occur at the induction motor terminals fed by PWM inverters. These overvoltages can reach 3 p.u or more and posse a threat for the motor insulation. Experimental results and simulations are used to study the dependence of voltage at the motor terminals from the application conditions (cable and motor parameters). A new algorithm for correction of the PWM, which reduce the motor terminal peak voltage under 2p.u, is proposed and tested successfully in different PWM schemes. Further more a method for calculation of the minimum allowed short time intervals between two consecutive pulses, is given and its results are confirmed from the experiment. Advantages of the new proposed PWM correction method are that it can be implemented at no additional costs, independently from the PWM mode (Sinusoidal PWM, Space Vector PWM, Discrete PWM) used、and without changing the performance of the drive. The application of this method improves the switching reliability of the drive.

Keywords: surge voltage, PWM, IGBT inverter drive, surge impedance, partial discharge.

1. Introduction

The application of IGBT-s as switching devices in the PWM variable speed drives (VSD) for the induction motor despite advantages in the drive performance brought some drawbacks too. One of them is the surge voltage problem. It consists in over voltages at the motor terminals and within windings and it is result of the combination of fast switching in the inverter and cable length over 10 m to the motor. These over voltages at 400V motors, in many cases exceed the partial discharge (PD) inception voltage level of the insulation, and reduce drastically its lifetime [9], [10]. Considering the wide application of the fast switching devices in drives for better performance and lower loss, the surge voltage problem exists in a wide range of industrial applications.

While high peak voltages at the motor terminals and their negative influence on the motor insulation have been reported and analyzed in different studies [3]- [5], [9], until now the solutions for reducing the peak voltage have not fulfilled the requirements for most industrial applications. Already proposed solutions require additional equipment as filters or adaptors with additional cost and space requirements.

In the literature there are few studies that recognize the influence of the DC link voltage and PWM parameters like carrier frequency, modulation method etc. on the peak voltage at the motor terminal. Even though such dependence exists, some of these parameters cannot be changed, or their change will influence drastically the drive performance considering current harmonics and noise.

In this paper based on the theoretical analysis, simulations and experiments it is proposed a new method for PWM correction which reduce the motor terminal voltage below the 2 p.u level without changing the drive performance. The reduced peak voltage level results below the partial discharge (PD) inception voltage of the motor insulation, preventing this way its occurrence. It is to be mentioned that the application of the correction method does improve drive reliability too.

In the section 2 we first analyze the conditions for the existence of danger overvoltages at the motor terminals and show a new method for calculation of the settling time of the voltage oscillations. Later in section 3, descriptions of modeling and computer simulations are shown. The accuracy of the computer model is evaluated by comparison with the experimental data. Then in section 4 we introduce the new method for correction of PWM and based on experimental tests, we show its effectiveness on surge voltage reduction. Finally in section 5 we discuss the issues of practical implementation and show the results of various tests on the drive performance.

2. Theoretical analysis of the surge voltage.

A power cable changes its behavior according to the frequency of the voltage applied to its terminals and its length. When the cable length is negligible compared to the voltage wavelength, it behaves like a lumped parameter circuit. This situation changes when the length of cable is comparable to the wavelength of the voltage applied. It occurs, for example in case of long power transmission lines or power cables used in variable frequency drives (VFD). In the last case the cable behaves as a distributed parameter circuit because of the high frequency voltage pulses from the inverter. Based on the traveling wave theory when the voltage wave arrives at the line end, a reflection occurs because of the difference between the cable and the motor surge impedances ($Z_{motor} >> Z_{cable}$). In case of IGBT inverters, the rise time about 0.1-0.2μs corresponds to a sinusoidal wave of about 1.6-3 MHz ($1/\pi t_r$). For common cable parameters (L and C) the speed of voltage wave propagation in the cable is about 150-180 m/μs (about half the speed of light). As a result the critical cable length when the full reflection occurs is about 10-12 m (1/4 of the voltage wave length). In the worst case considering the reflection coefficient between the cable and the motor $\gamma_r = \frac{Z_{motor} - Z_{cable}}{Z_{motor} + Z_{cable}} \approx 1$ the maximum peak voltage at the motor terminals would be near twice the inverter output. Because of the reflection phenomenon the line voltage at the motor terminals will oscillate with a period 4 times the propagation time of the voltage wave from the inverter to the motor ($4 \cdot \sqrt{L \cdot C} \cdot l$).

If the reflection phenomenon had been the only factor, the maximum peak voltage at the motor terminals would not exceed 2p.u (twice the DC link voltage level). It is an experimental fact that the voltage at the motor terminals can be as higher as 2.7 to 3p.u (sometimes even higher [11]). This is explained in the following:

Let us consider two consecutive pulses and a time interval between them. If the dwelling between two pulses is short, the voltage oscillations from the first pulse will not be extinguished when the second pulse arrives. Further more if the second pulse comes in phase with the existing oscillations, then the resonance will occur and the voltage peak can reach levels up to 3p.u or more.

We will illustrate the reflection and resonance phenomena by using an example of an ideal line (without loss).

In the following analysis for simplification, the reflection coefficients at the motor and the inverter terminals are considered respectively 1 and -1 (considering that $Z_{motor} >> Z_{cable} >> Z_{inv}$). The voltage waves are considered rectangular.

In Fig.1 are shown the terminal voltage waveforms in case of a falling pulse and a consecutive rising pulse after 2T (where T is the time interval the wave needs to travel the whole cable length). As seen from Fig.1 at t=0 it is supposed that the cable is charged and the transients are settled. An incident voltage (falling edge) tends to discharge the cable and is reflected several times at the motor and inverter terminals. Before voltage oscillations in the cable are settled a second pulse comes. This second rising edge pulse starts from the inverter terminal in the moment that the reflected wave of the first pulse (falling pulse) arrives for the first time at the same terminal (at t=2T).

For simplicity both reflected waves are analyzed independently from each other. In Fig.1 both waves are superimposed and a resultant voltage waveform is drawn at the motor terminals through the time. The above simplified analysis and the following diagrams help understanding the behavior of the cable in VFD and the phenomenon of overvoltage occurrence. Further more based on this analysis we calculate the minimum allowed time interval between two consecutive "on" pulses in order to prevent high peak voltages. This is shown in the following:

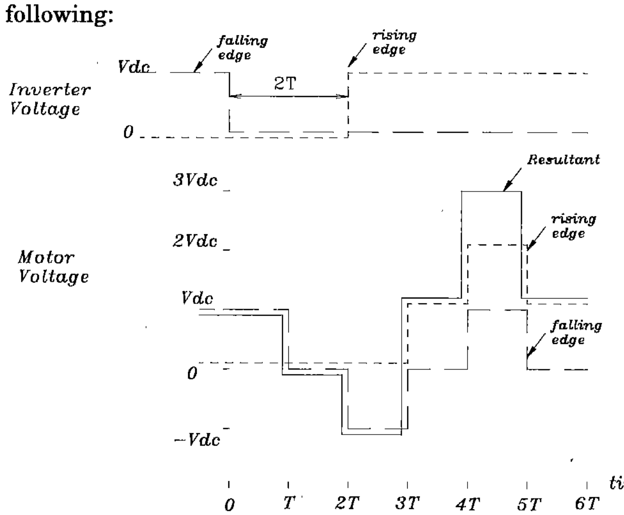

Fig.1. The voltage change at the motor against the time.

Let consider the reflection coefficients at the inverter and motor terminals respectively γ_1 and γ_2. Based on the theory of traveling waves, we have calculated the voltage at the motor terminals through the time in case of a step V input as following:

$$V_k = V_{k-1} + V \cdot (\gamma_2 \gamma_1)^k \cdot (1 + \gamma_2)$$
$$[(2k+1)T; (2k+3)T]\, k = 0,1,2,3,... \qquad (1)$$

Here we consider that the voltage at the motor terminals does not change in the interval $[(2k+1)T; (2k+3)T]$ where T is the propagation time of the voltage wave from the inverter to the motor. V_k and V_{k-1} are respectively voltages at the motor terminals right after an interval $[(2k+1)T; (2k+3)T]$ and that right before it.

If we consider further the losses in a very long line (where no reflections are present), considering that power released as heat should be equal to that lost from the pulse [7] we can find that:

$$V = V_0 \cdot e^{-\frac{r \cdot x}{2 \cdot Z}} \qquad (2)$$

Here: V_0 is the input step voltage and V is the voltage at distance x from the input terminal. Z and r are respectively the line surge impedance and its resistance. The motor terminal voltage oscillations decay as result of losses and reflections; therefore to calculate the settling time of oscillations from one single pulse both phenomena must be considered. From the voltage reflection formula (1) and the line losses one (2), we deduced the following formula (3) to calculate the time necessary until the voltage oscillations are damped to a given level ε:

$$t = (2 \cdot \log_a b + 1) \cdot \sqrt{L \cdot C} \cdot l$$
$$a = \gamma_1 \cdot \gamma_2 \cdot e^{-\frac{r \cdot l}{Z}} \qquad (3)$$
$$b = \left(\frac{2 \cdot \varepsilon}{(1 + \gamma_2)} \cdot e^{\frac{r}{2Z} \cdot l} \right)$$

t:settling time [sec]
γ_1:reflection coefficient at motor terminal. (absolute value)
γ_2:reflection coefficient at inverter terminal.
r:cable resistance [ohm/m]
L:cable inductance [H/m]
C:cable capacitance [F/m]
Z:cable surge impedance [ohm]
l:cable length [m]
ε:amplitude voltage in % after the oscillations are considered decayed.

We will use and discus further formula (3) in section 4, to calculate settling time of voltage oscillations.

3. Modeling, simulation and experimental assessment.

In PWM drives, at any instant of time (except zero states), if one leg of the inverter has its upper switch "on", the other two legs will have their lower switches "on". Therefore at any instant of time, one phase of the motor is connected in series with two other phases in parallel. The same is true for the cable too. The motor in this case can be represented as one phase equivalent (one phase of the motor in series with two other phases in parallel). During operation, the position of phases, switching on and off, will change. But there will be always one phase connected to one polarity of DC and the two others on the other polarity. The above-explained mode is called a differential mode, and cable and motor parameters measured in this mode are called differential mode parameters. We used this mode to model the cable and the motor.

The cable is modeled as a distributed parameter line (Bergeron model of the transmission line in Matlab). The model cannot represent correctly the frequencies very different from the fundamental frequency (where the cable parameter are measured). Especially the resistance is highly dependent from the frequency because of the skin effect, the inductance L changes slightly and capacitance C remains almost unaffected. These parameters are measured directly with an LCR meter at the frequency range of interest.

The motor model is represented by two parallel branches. One of them consists of a capacitor connected in series with a small resistance (this branch represent the motor at high frequencies) and the other consists of an inductance in series with a resistor (this branch represent the motor in low frequencies). Particularly important in our case is the first branch, which models the capacitive behavior of the motor at the high frequencies. The capacitive behavior of the motor can be seen from measurements in Tab.2.

The differential mode parameters, measured with a LCR meter, for a 3x5.5mm^2 cable and an 11kW, 4-pole motor (Fuji Electric Co.) are given in Tab. 1 and Tab. 2 respectively, in the frequency range from 10kHz to 2MHz.

Tab.1. Cable parameters.

f[MHz]	0.01	0.02	0.04	0.1	0.2	0.4	1	2
C[pF/m]	59.4	59.3	59.3	59.1	59.3	59.3	59.2	59.1
L[nH/m]	499	484	459	438	425	415	407	404
R[mΩ/m]	5.7	9.1	13.3	25.9	37.1	53.6	91.1	126

Tab.2. Motor parameters.

f[MHz]	0.01	0.02	0.04	0.1	0.2	0.4	1	2
C[nF]	-	-	-	-	1.52	1.13	1.35	2.7
L[mH]	1.41	1.07	0.89	1.3	-	-	-	-
R[Ω]	14.6	23.0	64.8	570	556	144	9.6	4.7

The values from Tab. 1 and 2 used in simulation are taken from Tab.1 and 2 at 2Mhz and 1Mhz respectively:
Cable: R=126 ohm/km, L=0.404mH/km, C=59.1nF/km.
Motor: R_c=9.6ohm, C=1.35nF, R_l=0.14ohm, L=41mH.

In Fig.2 are compared voltage waveforms at the motor terminals from the experimental data with those from simulations. In simulations are included the cable and the motor model, with parameters shown above. The IGBT drive is not included. Instead, in order to get the same conditions with the experiment, we used the experimental data, recorded at the inverter terminal, as input in simulations too.

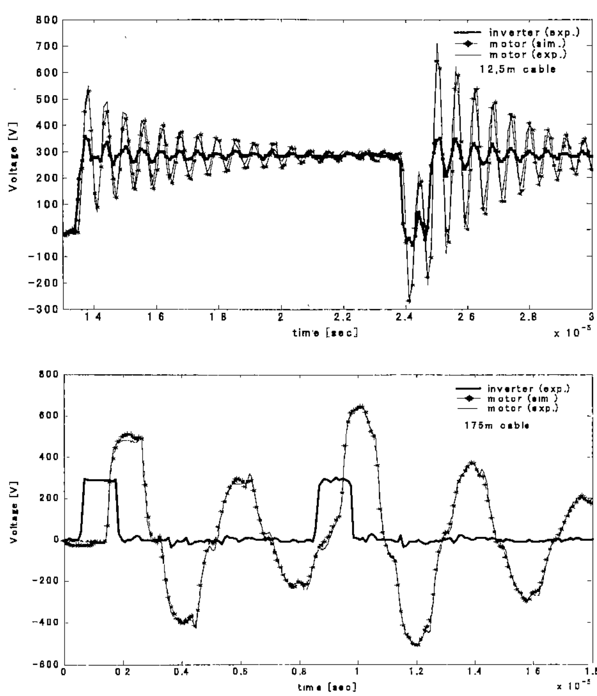

Fig.2. Measured inverter output, and measured and simulated motor terminal voltage.
(Upper 12.5m and lower 175m cable length.)

It is obvious from Fig.2 that the simulated motor voltage waveform agrees very well with that recorded from the experiment.

4. PWM correction method for reduction of the surge voltage at the motor.

In the analysis of the surge voltage at the motor terminals, given in section 2, we concluded that the resonance phenomenon is the reason of peak voltages higher than 2p.u. Therefore in order to prevent these dangerous peak voltages, we have shown that a minimum allowed time interval between consecutive pulses must be set. We have given also in section 2 a new formula (3) for calculation of this minimum allowed time interval between two consecutive pulses and shown that it must be long enough to allow voltage oscillations to be damped before the next pulse arrives.

Fig.3 illustrates the principle of this correction method and the respective compensation. As seen in Fig.3 the PWM waveform of the line voltage is changed after correction such that the time interval between pulses shorter than the allowed minimum are set at the minimum level or eliminated (depending on how short they are). The error made is carried to the next coming period. The maximum error between the averages of the corrected and the non-corrected voltage references taken within two or more carriers is less than (1-min)/2. The error taken over the period of time that the reference resides between min and 1 is zero in any case.

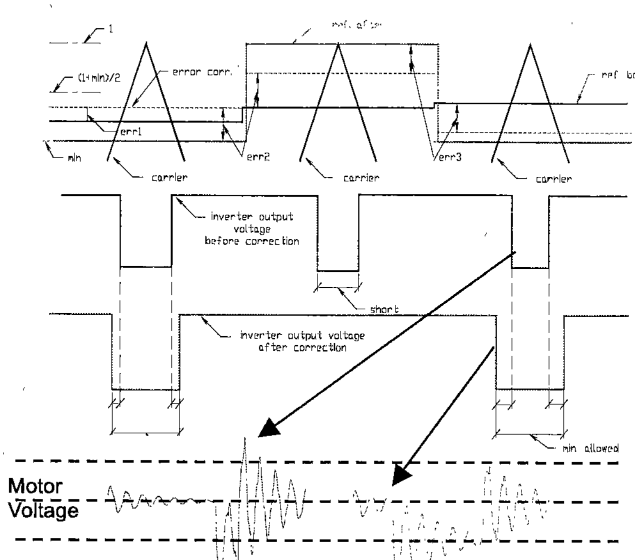

Fig.3. PWM before and after correction.

From the analysis of the PWM synthesis a short time interval between two consecutive pulses in the line voltages occurs when the reference voltage command approaches the top level (1 p.u positive or negative) of the carrier. Therefore the method is applied in all cases when the voltage reference enters in the region where short dwelling is generated.

As shown in Fig.3, if the voltage reference lie between min. and 1 p.u level it will be corrected to level min. if less than (1+min)/2 and to level 1 if greater than (1+min)/2. The error, which is the difference between the voltage reference before correction with that after correction, is added to the next update of the voltage reference. This way, the average voltage level will be compensated for changes made by the correction Fig4.

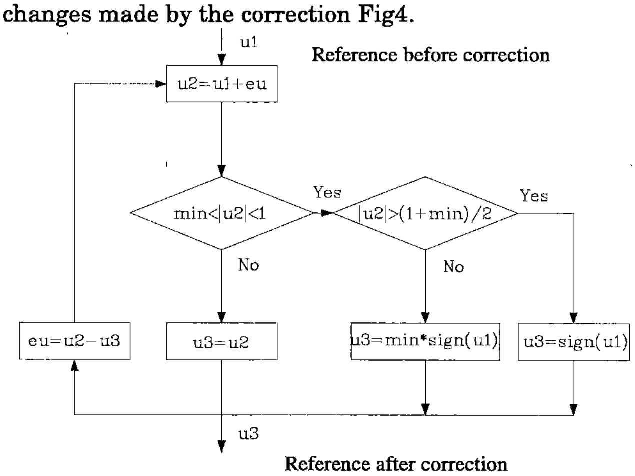

Fig.4. Block diagram of the correction algorithm.

It is obvious from the PWM waveform that only short intervals corresponding to the min. level are generated and the error is compensated properly. The min. level allowed of the voltage reference is calculated for the cable and motor parameters from formula (3). It should be mentioned that the reflection coefficient at the motor terminal can be measured from the reflection of a step voltage given from the inverter as γ_2=(Vpeak-Vstep)/Vstep. Where the Vstep is the voltage step measured at the inverter terminal and Vpeak is that correspondent to the motor terminal. This coefficient depends on the cable and motor surge impedances and if known, it can be determined from those too. As for the reflection coefficient at the inverter, it can be approximated as 1 without any practical error.

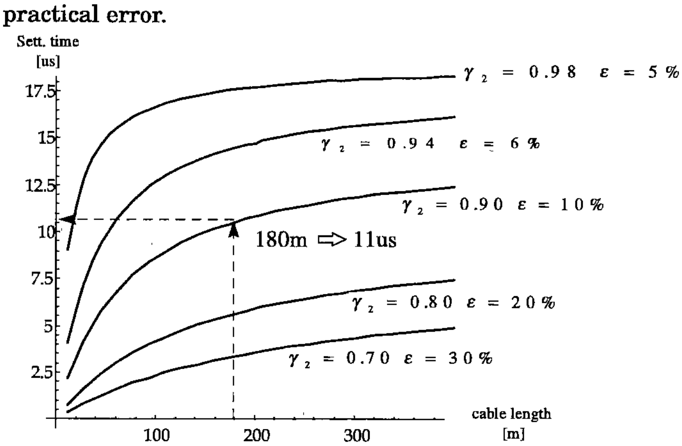

Fig.5. Settling time of oscillations against cable length.

Here:

$L = 0.4\,mH\ /\ km$

$C = 59\,nF\ /\ km$

$r = 126\Omega\ /\ km$

$Z = 82\Omega$

$\gamma_1 = 1.0$

t : settling time [sec]
γ_1: reflection coef. at mot.
γ_2: reflection coef. at inv.
r : cable resistance [ohm/m]
L: cable inductance [H/m]
C : cable capacitance [F/m]
Z : cable surge impedance [ohm]
l : cable length [m]
ε : settled voltage [%]

In Fig.5 are shown the characteristics plotted from eq.3 against the cable length, for different values of the reflection coefficient at the motor terminals. From these curves it is seen that the settling time of oscillations increase very fast with cable length in the region 10-100m. After 200m the increase is much slower. This is because losses (skin effect) increase proportionally with the cable length. On the other hand even though short cables have lower losses, the higher number of reflections at the motor terminal influence the decay of voltage oscillations. We can say that in short cables, the large number of reflections plays the most important role in voltage oscillations decay, but in long cables, losses are the predominate factor.

Finally it is important to be noticed that after calculation of the settling time (min. allowed time between two pulses) according to eq. 3 or the graph in Fig.5 the dead time setting should be taken in consideration to the calculated min. dwell value. The final result is set in the drive controller as a parameter and for a given motor, practically depends only on the cable length.

5. Implementation and drive performance

The correction algorithm is implemented in the drive controller (TMS320 DSP). The algorithm is inserted right after the calculation of the voltage reference from the controller, and before the voltage reference (formatted) is sent to the FPGA for the comparison with the carrier wave. A simple block diagram is shown in Fig.6 below:

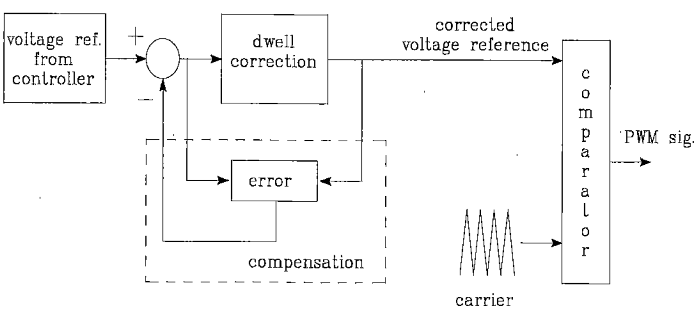

Fig.6. Block-diagram for application of the PWM correction method.

The correction block shown in the diagram above compensates the error from the correction in the next coming carrier period.

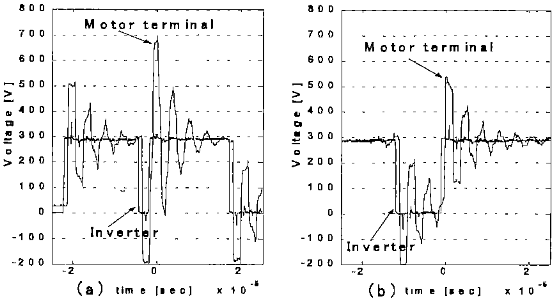

Fig.7. Max. peak line voltage at the motor terminal for a 175m cable. (a-without correction 710V and b-with correction min. dwell 11us 530V.)

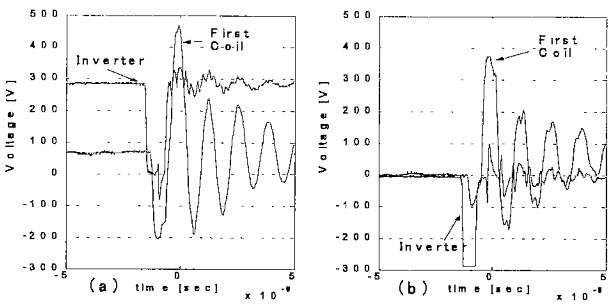

Fig.8. Max. peak first coil motor voltage for a 50m cable. (a-without correction 476Vand b-with correction min. dwell 8us 378V.)

For the assessment of the correction method, experiments were conducted in cases with and without correction and voltage waveforms were recorded. The voltage between the motor terminals U and V is shown in (Fig.7) and the voltage of the first coil, between its terminals U and S1, is shown in (Fig.8). U is the motor phase terminal and S1 represent the other terminal of the first coil of phase U. There are 4 coils connected in series for each phase. To measure the voltage waveform of the first coil we used a special built motor, which had 4 coils in series per phase and all those terminals accessible from outside. Experiments were conducted with carrier frequency 10kHz, for different modulation methods as Sinusoidal PWM, Space Vector PWM, Discrete PWM and for different conditions of speed and load, with and without dead time compensation. Maximum peak voltage reduction was verified for different cable lengths from 12,5 to 175m. In Fig.7 and 8 are shown only two cases for 175m and 50m cables.

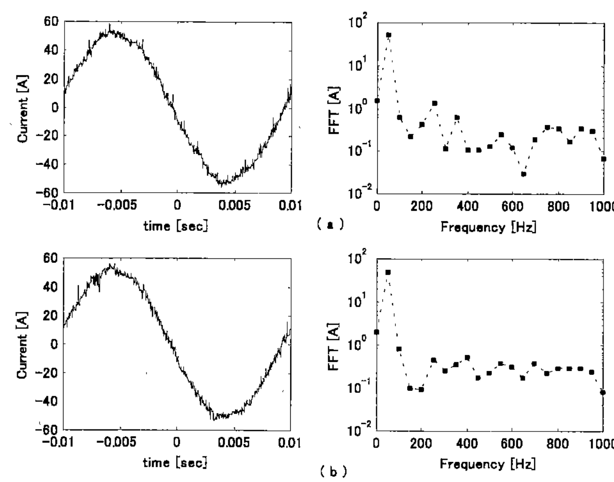

Fig.9. Current waveform at 85% load (9.5kW) and the respective harmonics content.
(a-without correction and b-with correction min. dwell 10us.)

In Fig.9 are shown current waveforms and their respective harmonic contents (from FFT analysis) measured in both cases (with and without correction algorithm). It is seen that the current waveform has no distortion from the applied correction algorithm.

To evaluate the noise level for the corrected PWM method, the noise was measured for different modulation methods, in different speeds, with and without correction. In all cases the spectrum of the noise was also analyzed. The noise level change was negligible as seen from Tab.3 below. The experiment was conducted in an experimental room. The ambient noise level before and after the experiment (when the motor is switched off) was 62dB. During the measurement a type A (flat) filter was used and the measuring equipment was placed in a distance 1m from the motor. During the experiment no load was applied at the motor.

Tab.3. Noise level in [dB]

PWM Mode	@ 1000 rpm	@ 1300 rpm	@ 1500 rpm	@ 1800 rpm	Pulse Correction
SPWM	66.0	71.5	73.5	77.5	No correct
	66.0	72.0	73.5	77.7	10us
	66.0	73.0	73.8	77.9	15us
SVPWM	65.0	70.0	73.5	77.5	No correct
	65.0	71.5	74.0	77.6	10us
	65.0	74.0	74.5	77.6	15us
DPWM	70.0	71.5	73.5	77.5	No correct
	70.0	71.5	73.5	77.7	10us
	70.0	71.5	73.8	77.8	15us

In general the influence of the correction algorithm becomes stronger when the reference voltage resides for a longer time between 1pu and min-pu where the correction take place.

Vibration of the motor was measured in cases without and with correction. Comparing both cases, we concluded that there was no change in the motor vibrations. The spectrum of the vibrations has two peaks at 9.8kHz and at 5.9kHz in all cases. These frequencies correspond to carrier frequency and sampling frequency of the reference voltage respectively.

6. Conclusions

In this paper a new algorithm for reduction of the surge voltage at the motor terminals by PWM correction is proposed. Implementation and experimental test have shown that it reduces the motor terminal voltage from 3 p.u to less than 2 p.u (2 times the DC link voltage level). Furthermore it does not change the drive performance and there are no additional costs for its implementation. Because it eliminates very short time intervals between two consecutive pulses, the method improves the reliability of the drive too. It is particularly advised that the method be applied in 400 V, IGBT variable speed drives.

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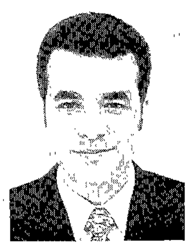

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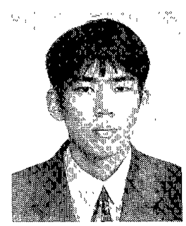

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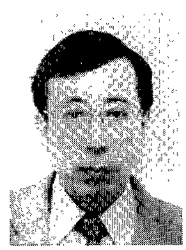

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