Fast Logical Location of Faults in Large Analog Electronic Circuits

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This paper presents a method for fast off-line logical location of faults in analog electronic circuits at the sub-network level and verifies its practical diagnosability. The proposed approach breaks through the previous limitation that all torn terminals (incident nodes) must be accessible and that the mutual-testing method must be utilized to locate the faulty sub-networks. As far as the diagnosability is concerned, its application is more extensive than the unified decomposition approach. Therefore it better satisfies the engineering needs.

Keywords: analog circuit, sub-network, off-line fault diagnosis, intersected-torn rule, logical location

1. Introduction

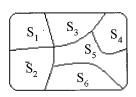
In general, analog electronic circuits are diagnosed at offline state. Topological constructions of practical analog electronic circuits should almost never be satisfied with the conditions of diagnosability for the number of faulty elements k > 2 when applying node-faulty equations to locate the faulty element ^[1]. Other diagnosis methods have similar conclusions $[^{2}, ^{3}]$. Therefore, fault diagnosis theory at the sub-network level has received special attention recently ^[4]. However, up to now the above methods for diagnosing at the sub-network level almost limit to all torn nodes (incident nodes) to be accessible and apply the mutual-testing method to locate the faulty sub-networks. Apparently, these restraining conditions are comparatively rigorous and limit its applications ^[1].

This paper presents a new off-line torn search approach at sub-network level that breaks through the above-restrained conditions, and applies the logical diagnostic function or logical diagnostic matrix to locate the faulty sub-network. Here we also verify in detail its diagnosability as compared with the unified decomposition approach.

2. Intersected-Torn Search Approach

 $\langle 2\cdot 1\rangle$ Intersected-torn rules According to the physical constructions and technological requirements of electronic circuits, we can divide a network N into many subnetworks S_i (i=1, 2,...), as shown in Fig.1 (a). If an incident node between two sub-networks can be described as a line, the incidence relations between sub-networks can be described as a torn diagnostic graph TP, as shown in Fig.1 (b).

For the first tearing T_1 in Fig.1 (b), TP can be performed along the boundary between $\{S_1, S_3\}$ and $\{S_2, S_4, S_5\}$. Then, we can obtain the sub-networks sets N_1^1 and \hat{N}_1^1 , as shown in Fig.2 (a) and (b). The second tearing T_2 can be performed



 S_3 S_4 S_5 S_5 S_5 S_6 S_7 S_9 S_9

(a) Network N

Fig. 1. Network connection

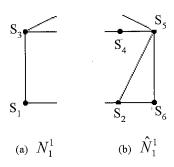


Fig. 2. First tearing T_1

along the boundary between $\{S_1, S_2\}$ and $\{S_3, S_5, S_6\}$. We can obtain the sub-networks sets N_1^2 and \hat{N}_1^2 , as shown in Fig.3 (a) and (b). By repeating the tearing, we can obtain the sub-networks sets N_1^1 , \hat{N}_1^1 , N_1^2 , \hat{N}_1^2 , and so on. By selecting the accessible nodes correctly for these sub-networks [4,5], we can judge whether or not each sub-network has a fault.

Let N be the linear network in Fig.1 (a), tearing N into two sub-networks: N_1^1 and \hat{N}_1^1 . In N_1^1 (as shown in Fig.4),

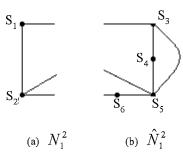


Fig. 3. Second tearing T_2

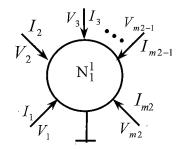


Fig. 4. Sub-network

the torn nodes consist of the inaccessible subset TT ($tt \in TT$) and the accessible subset MT ($mt \in MT$), and the un-torn accessible nodes by GM ($gm \in GM$). Then the following equations can be obtained.

$$m = gm + mt$$
(1)

$$m_2 = tt + mt$$
(2)

where m and m_2 are respectively the number of accessible nodes and the number of torn nodes in N_1^1 . If N_1^1 is connected and not mutual-coupled with \hat{N}_1^1 in Fig.4, the node-voltage equation of N_1^1 is expressed as

$$\begin{bmatrix} Y_{1n} \end{bmatrix} \begin{bmatrix} V_{1n} \end{bmatrix} = \begin{bmatrix} I_m \end{bmatrix} + \begin{bmatrix} I_{ts} \\ 0 \end{bmatrix} \qquad (3)$$
 where,
$$\begin{bmatrix} V_{1n} \end{bmatrix} = \begin{bmatrix} V_{TT} & V_{MT} & V_{GM} & V_{TI} \end{bmatrix}^T,$$

where, $\begin{bmatrix} \mathbf{r}_{1n} \end{bmatrix} = \begin{bmatrix} \mathbf{r}_{TT} & \mathbf{r}_{MT} & \mathbf{r}_{GM} & \mathbf{r}_{H} \end{bmatrix}$ $\begin{bmatrix} I_{m} \end{bmatrix} = \begin{bmatrix} 0 & I_{MT} & I_{GM} & 0 \end{bmatrix}^{T},$

$$\begin{bmatrix} I_m \end{bmatrix} = \begin{bmatrix} 0 & I_{MT} & I_{GM} \\ & & & \end{bmatrix}$$

 $\begin{bmatrix} I_{ts} \end{bmatrix} = \begin{bmatrix} I_{TT} & I_{SM} \end{bmatrix}^T.$

Here $[Y_{1n}]$ is determined by the nominal values of fault-free elements in N_1^1 and $[I_{SM}]$ is the vector of unknown currents at the torn accessible nodes. Eliminating the vector of internal node-voltage $[V_{II}]$ from (3) and rearranging some elements of $[V_{1n}]$, we obtain the following equation.

$$\begin{bmatrix} Y_1 & Y_2 \\ Y_3 & Y_4 \end{bmatrix} \begin{bmatrix} V_m \\ V_i \end{bmatrix} = \begin{bmatrix} I_m \end{bmatrix} + \begin{bmatrix} I_{ts} \\ 0 \end{bmatrix} \qquad (4)$$

where
$$\begin{bmatrix} V_m \end{bmatrix} = \begin{bmatrix} V_{MT} & V_{GM} \end{bmatrix}^T$$
: the known vector, $\begin{bmatrix} V_i \end{bmatrix} = \begin{bmatrix} V_{TT} & V_{II} \end{bmatrix}^T$: the unknown vector.

Taking the measured voltage values of accessible node $[V_m]$ into (4) when $m = m_2$, the unknown vector $[I_{ts}]$ can be calculated by (4). If N_1^1 is fault-free, $[I_{ts}]$ should satisfy

the Kirchhoff current law, i.e.

$$\sum_{i=1}^{m_2} I_{ts_j} = 0 (5)$$

If N_1^i of the *i*th-time tearing is satisfied with (5), all subnetworks of N_1^i are fault-free, and its logical value is 0, i.e. $TS(N_1^i)$ =0. Otherwise, one or more sub-networks of N_1^i may be faulty and its logical value is 1, i.e. $TS(N_1^i)$ =1. Therefore, each sub-network can be associated with a logical variable that takes the value 0 if the sub-network is fault-free and 1 if it is possibly faulty.

Although a given electronic circuit may contain several hundred components, it is reasonable to assume that at most two or three components have failed simultaneously. So our research is based on the assumption that the number of faulty sub-networks f should never be greater than 3. Namely, we shall derive the intersected-torn searching rules under $f \leq 3$ [6]

DEFINITION If a network N may be divided into m subnetworks, any two or any three sub-networks can consist of a pseudo-two sub-networks S_{ijk} respectively. The sum of the pseudo sub-networks is obviously $C_m^2 + C_m^3$.

Now illustrated with Fig.2, we investigate how the information of non-faulty sub-networks or non-faulty pseudo sub-networks can be obtained from the logical variables in each tearing. Let the logical variables in the first tearing T_1 for Fig.2 be $TS(N_1^1)=0$ and $TS(\hat{N}_1^1)=1$. If f=1, the nonfaulty sub-networks should be s_1 and s_3 and the possibly faulty sub-networks should be S_2 , S_4 , S_5 and S_6 , respectively. If f = 2, the non-faulty and the possibly faulty pseudo-two sub-networks should be $S_{12},\ S_{13},\ S_{14},\ S_{15},\ S_{16},\ S_{23},\ S_{34},\ S_{35},\ S_{36}$ and S_{24} , S_{25} , S_{26} , S_{45} , S_{46} , S_{56} . If f = 3, we can also obtain the information about the pseudo-three sub-networks (to be omitted). The above method for obtaining information about sub-networks and pseudo sub-networks can also be applied to the second tearing T_2 , the third tearing T_3 and so on. According to this logical reasoning process, we can present four rules for tearing a network N under $f \le 3$ as follows:

RULE 1 Any two sub-networks S_i and S_j of network N have been torn at least once, during cross tearing of k times during which the sub-network set N_1^i or \hat{N}_1^i (i=1, 2, ... k) includes one and only one of the two sub-networks S_i or S_j .

RULE 2 Any two pseudo-two sub-networks S_{ij} and S_{pt} of N

have been torn at least once, during cross tearing of k times during which N_1^i or \hat{N}_1^i (i=1, 2, ... k) includes one and only one of the two pseudo-two s_y or s_{pt} .

RULE 3 Any two pseudo-three sub-networks s_{ijk} and s_{pqr} of N have at least been torn once, during cross tearing of k times during which N_1^i or \hat{N}_1^i (i=1, 2, ... k) includes only one of the two pseudo-three s_{ijk} or s_{pqr} but not the other one.

RULE 4 During cross tearing of k times, any three of the sub-networks s_i , s_j , s_k of N have been torn at least three times which make them belong to N_1^i or \hat{N}_1^i separately.

Obviously, rules 1 and 2 are in need of $f \le 2$ and rules 1-4 are in need of $f \le 3$.

(2.2) Logical Location of faulty sub-networks

Network N has been torn k times satisfying the above rules, the fault of the sub-networks should be located by LD_f (f=1,2,3) referred to as the logical diagnostic matrix. The matrix LD_f is formed as below. The rows of LD_f correspond to the number of tearings T_i (i=1, 2, ..., k), and the columns of LD_f correspond to the sub-networks under f=1 or to pseudotwo sub-networks under f=2 or to pseudo-three sub-networks under f=3. The elements of LD_f are 0 or 1. If the sub-networks or the pseudo sub-networks correspond to the f=1 column of the matrix in f=1 tearing, then it is judged to be fault-free, the element f=10 of the matrix is 0, and 1 otherwise.

Now the matrix LD_f formation is illustrated with the first tearing T_I of Fig.2. If N_1^1 is judged non-faulty, then all subnetworks in N_1^1 are non-faulty. Otherwise, \hat{N}_1^1 is faulty. Some sub-networks in \hat{N}_1^1 may be faulty. The matrix LD_f formation is discussed as follows:

1) If there is a sub-network fault in networks N (f = 1), then non-faulty sub-networks are S_1 , S_3 and possible faulty sub-networks are S_2 , S_4 , S_5 , S_6 . The elements of the matrix LD_1 are deduced as follows:

$$LD_{1} = \begin{bmatrix} s_{1} & s_{2} & s_{3} & s_{4} & s_{5} & s_{6} \\ 0 & 1 & 0 & 1 & 1 & 1 \\ & & \vdots & & & \end{bmatrix}$$

2) If there are two faulty sub-networks in networks N (f=2), then the non-faulty pseudo-two sub-networks are S_{12} , S_{13} , S_{14} , S_{15} , S_{16} , S_{23} , S_{34} , S_{35} , S_{36} and possible faulty pseudo-two sub-networks are S_{24} , S_{25} , S_{26} , S_{45} , S_{46} , S_{56} . The matrix LD_2 is formed as below

$$LD_2 = \begin{bmatrix} s_{12} & s_{13} & s_{14} & s_{15} & s_{16} & s_{23} & s_{24} \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & * \\ & & & \vdots & & & \vdots & & & & \end{bmatrix}$$

In addition to the logical diagnostic matrix, the faulty subnetworks could be also located by $FD_f(f=1, 2, 3)$ referred to as the logical diagnostic function.

$$FD_{i} = \left(\bigcap_{i=1}^{k} T_{f}^{i}\right) \cap \left(\bigcap_{i=1}^{k} \hat{T}_{f}^{i}\right) \qquad (6)$$

where T_f^i or \hat{T}_f^i (f=1, 2, 3; i=1, 2, 3...k) is referred to as the logical tearing function at T_t tearing.

$$T_f^i = s_{i1} \cap s_{i2} \cap \cdots \cap s_{im} \quad \cdots$$
 (7)

$$\hat{T}_f^i = \hat{s}_{j1} \cup \hat{s}_{j2} \cup \cdots \cup \hat{s}_{jm} \quad \dots \tag{8}$$

where S_{j1} , S_{j2} , ... S_{jm} are labels of the sub-networks under f=1 or of pseudo sub-networks under f=2,3 judged as fault-free at T_i tearing, and \hat{S}_{j1} , $\hat{S}_{j2} \cdots \hat{S}_{jm}$ otherwise.

It is easily proved that the following conclusions are correct. (1°) If and only if only one of these matrices $LD_f(f=1,2,3)$ contains only one column in which all elements are 1 and the remaining columns otherwise. The f corresponding to this matrix correctly represents the number of faulty subnetworks, and this column correctly represents the fault location. (2°) Functions FD_f (f=1,2,3) can be simplified by Boolean Algebra. Therefore, if and only if only one of these simplified functions contains all components in which only one must be a complemented term \hat{S}_{jx} , then the number and the locations of faulty sub-networks should be respectively represented by the f and the \hat{S}_{jx} in the logical diagnostic function FD_f .

3. Diagnosability for Some Typical Circuits

In this section, we shall compare the diagnosability of the intersected-torn search approach compared with the unified decomposition approach ^[2,3] with some typical circuits. It is emphasized that the latter requires all incident nodes to be accessible, and the former has no such requirement ^[4].

1) A ladder circuit, such as a Chebyshev filter should be a good example. We examine a five-section Chebyshev filter circuit simply, as shown in Fig. 5.

According to the matrices D_1 and D_2 which are formed by the unified decomposition approach in Reference [3], there are some identical column sets in it, such as $C_1 = \{s_2, s_{12}\}$, $C_2 = \{s_4, s_{45}\}$, $C_3 = \{s_{13}, s_{23}\}$ and $C_4 = \{s_{34}, s_{35}\}$. Thus, the maximum number of diagnosable faulty sub-networks f should be 1. Then the number f by the intersected-torn search approach for Fig.5 is 2. The verifying process is omitted.

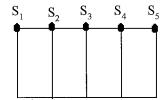


Fig. 5. Chebyshev filter TP

- 2) Distribution feeder circuits. A diagram of a circuit is shown in Fig.6. According to the D_1 and D_2 matrices (to be omitted) by the unified decomposition approach, there are some identical column sets in it, such as $C_1 = \{S_2, S_{12}\}$, $C_2 = \{S_3, S_{34}\}$, $C_3 = \{S_6, S_{56}\}$ and $C_4 = \{S_7, S_{78}\}$. We can verify easily that the maximum number of faulty sub-networks diagnosed is 1. But the number of tearing by the proposed approach is 6 under $f \leq 2$.
- 3) Cluster circuit. An example with two clusters is shown in Fig.7. It is easily verified that the maximum number of faulty sub-networks diagnosed by the unified decomposition approach is f=1, because there are some identical column sets in it, such as $C_1 = \{S_2, S_{24}, S_{25}\}$, $C_2 = \{S_3, S_{36}, S_{37}\}$. However, the number of tearing is never greater than six under $f \leq 2$ by the proposed approach. The verifying process is omitted.

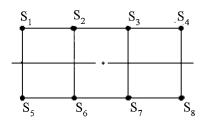


Fig. 6. Distribution feeder circuit TP

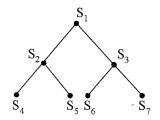


Fig. 7. Cluster circuit TP

4. Example

Fig.8 shows a dc source electronic circuit. According to the construction of this circuit, it can be divided into five subnetworks. Its torn-diagnostic graph TP is identical with Fig.5. If the number of faulty sub-networks is two ($f \le 2$), then we have an intersected-torn search scheme satisfying the tearing rules as follows:

$$T_1: \quad N_1^1 = \{s_4, s_5\}, \qquad \qquad \hat{N}_1^1 = \{s_1, s_2, s_3\};$$

$$T_2: \quad N_1^2 = \{s_1, s_2\}, \qquad \qquad \hat{N}_1^2 = \{s_3, s_4, Ss_5\};$$

$$T_3: \quad N_1^3 = \{s_1\}, \qquad \qquad \hat{N}_1^3 = \{s_2, s_3, s_4, s_5\};$$

$$T_4: \quad N_1^4 = \{s_5\}, \qquad \qquad \hat{N}_1^4 = \{s_1, s_2, s_3, s_4\}.$$
Let sub-networks s_2 and s_5 be faulty, the logical variables of

Let sub-networks s_2 and s_5 be faulty, the logical variables of these sub-networks set N_1^1 , \hat{N}_1^1 , N_1^2 , \hat{N}_1^2 , \hat{N}_1^3 , \hat{N}_1^3 , \hat{N}_1^3 , N_1^4

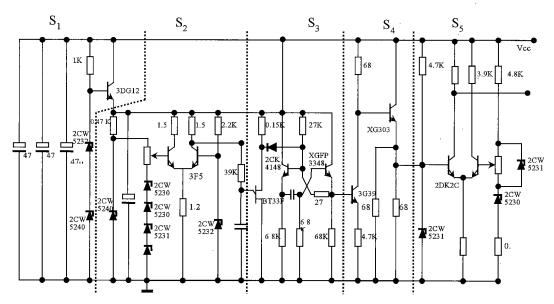


Fig. 8. Electronic circuit of a dc source

and \hat{N}_1^4 should be following [5,7]:

$$T_1$$
: TS(N_1^1)=1, TS(\hat{N}_1^1)=1,

$$T_2$$
: TS $(N_1^2)=1$, TS $(\hat{N}_1^2)=1$,

$$T_3$$
: TS $(N_1^3)=0$, TS $(\hat{N}_1^3)=1$,

$$T_4$$
: TS $(N_1^4)=1$, TS $(\hat{N}_1^4)=1$.

Based on the above logical variables, we can establish the logical diagnostic matrices $LD_f(f=1,2)$ as follows:

$$LD_2 = \begin{bmatrix} s_{12} & s_{13} & s_{14} & s_{15} & s_{23} & s_{24} & s_{25} & s_{34} & s_{35} & s_{45} \\ 0 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 1 & 0 \\ 0 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix}$$

According to the above logical diagnostic matrices, the faulty sub-networks S_2 and S_5 can be identified. It is clear that this result is all just the same as the assumed condition. In addition to the logical diagnostic matrix, the faulty subnetworks could also be located by $FD_f(f=1,2)$ as follows:

$$FD_{1} = S_{1} \cap (\widehat{S}_{2} \cup \widehat{S}_{3} \cup \widehat{S}_{4} \cup \widehat{S}_{5}) \cap (\widehat{S}_{1} \cup \widehat{S}_{2}$$

$$\cup \widehat{S}_{3} \cup \widehat{S}_{4} \cup \widehat{S}_{5}) \cap (\widehat{S}_{1} \cup \widehat{S}_{2} \cup \widehat{S}_{3}$$

$$\cup \widehat{S}_{4} \cup \widehat{S}_{5}) \cap (\widehat{S}_{1} \cup \widehat{S}_{2} \cup \widehat{S}_{3} \cup \widehat{S}_{4} \cup \widehat{S}_{5})$$

$$= S_{1} \cap (\widehat{S}_{2} \cup \widehat{S}_{3} \cup \widehat{S}_{4} \cup \widehat{S}_{5})$$

$$\begin{split} FD_2 &= (S_{12} \cap S_{13} \cap S_{23} \cap S_{45}) \cap (S_{12} \cap S_{34} \\ &\cap S_{35} \cap S_{45}) \cap (S_{12} \cap S_{13} \cap S_{14} \\ &\cap S_{15}) \cap (S_{12}S_{13} \cap S_{14} \cap S_{23} \cap S_{24} \\ &\cap S_{34}) \cap (\widehat{S}_{14} \cup \widehat{S}_{15} \cup \widehat{S}_{24} \cup \widehat{S}_{25} \\ &\cup \widehat{S}_{34} \cup \widehat{S}_{35}) \cap (\widehat{S}_{13} \cup \widehat{S}_{14} \cup \widehat{S}_{15} \\ &\cup \widehat{S}_{23} \cup \widehat{S}_{24} \cup \widehat{S}_{25}) \cap (\widehat{S}_{23} \cup \widehat{S}_{24} \\ &\cup \widehat{S}_{25} \cup \widehat{S}_{34} \cup \widehat{S}_{35} \cup \widehat{S}_{45}) \cap (\widehat{S}_{15} \\ &\cup \widehat{S}_{25} \cup \widehat{S}_{35} \cup \widehat{S}_{45}) \\ &= S_{12} \cap S_{13} \cap S_{14} \cap S_{15} \cap S_{23} \cap S_{24} \cap \widehat{S}_{25} \\ &\cap S_{34} \cap S_{35} \cap S_{45} \end{split}$$

According to the above logical diagnostic function FD_1 and FD_2 , it is clear that the faulty sub-networks S_2 and S_5 can be identified.

This example shows that the faulty sub-networks can be identified by 4 tearings with the proposed approach. However, the unified decomposition approaches in Reference 2 and 3 cannot identify the faulty sub-networks due to equivocal diagnosis. It is also indicated that the proposed approach can diagnose large electronic circuits effectively.

5. Conclusions

In this paper, a new off-line intersected torn node search approach for fault diagnosis of analog electronic circuits at the sub-network level is proposed. This approach breaks through the limitation that all torn terminals must be accessible, and applies the computing-self-testing ways of the logical diagnostic function or logical diagnostic matrixes to judge whether the sub-network is faulty. An advantage is that the proposed approach reduces the range of fault diagnosis of large electronic circuits and the computing time of fault diagnosis. Another advantage is that the approach raises the re-applying efficiency of accessible nodes. Therefore, the proposed approach is fast and efficacious. In particular, some typical circuits, such as ladder circuits, distribution feeder circuits and cluster circuits and so on, are easily verified that the maximum number of faulty sub-networks diagnosed by the unified decomposition approach should be f=1. However, the maximum number by the proposed approach can be f=2. Thus, this application is more extensive than the unified decomposition approach. Therefore, the proposed method better satisfies the engineering needs for sub-network level.

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