Paper

Design of a Ring-Type SC DC-DC Converter with Bootstrapped Gate Transfer Switches

Kei Eguchi* Member Toru Tabata* Non-member
Hongbing Zhu** Member Fumio Ueno*** Member
Ichirou Oota* Member Takahiro Inoue**** Member

In this paper, a ring-type SC DC-DC converter with novel bootstrapped gate transfer switches is proposed. The bootstrapped gate transfer switches are used to achieve higher efficiency. In the proposed bootstrap circuit, maximum voltage of the power converter is charged to a capacitor via maximum circuits constructed with diodes. By connecting the charged-capacitor between the gate terminals of power-switches and the output terminal of the maximum circuit, the bootstrap circuit avoids the threshold voltage drop of power-switches. Concerning the DC-DC converter designed by a 1.2 μm CMOS technology, SPICE simulations are performed to investigate the characteristics of the circuit. The SPICE simulations show that the efficiency of the DC-DC converter with proposed bootstrap circuits is more than 90 % when the output load R_o satisfies $R_o > 200\Omega$. When $R_o = 100\Omega$, the proposed circuit can improve efficiency up to 8.7 % of a conventional converter. The validity of the circuit design for the bootstrap circuit is also confirmed by experiments.

Keywords: DC-DC converters, switched-capacitor circuits, inductor-less circuits, discrete-time circuits, analog circuits

1. Introduction

Recently, power conversion circuits designed by using switched-capacitor (SC) techniques [1]~[17] attract many researchers' attention since they require no magnetic elements such as inductors. The power conversion circuits using magnetic elements cause possibility of faulty operation for neighboring circuits. For this reason, several types of SC power converters have been proposed [1]~[17]. For example, Mak et al. realized a series-parallel type AC-DC converter [6] and we proposed a cell-network type DC-DC converter [13]. Only to control the timing of clock pulses, these circuits can provide step-up and step-down voltages.

The SC power converters consist of only power-switches, capacitors, and clock-pulse generators. Among others, the design of power-switches is important. To achieve high efficiency and small number of power-switches, the gate terminals of power-switches must be driven by higher voltages than that of the source terminals. For this reason, we focused on bootstrapped gate transfer switches.

In this paper, a ring-type SC DC-DC converter [1] with novel bootstrapped gate transfer switches is proposed. The ring-type SC DC-DC converter is one of the most efficient converters which can provide step-up and step-down voltages. In the proposed bootstrap circuit, maximum voltage of the power converter is charged to a capacitor via maximum circuits constructed with diodes. By connecting the charged-capacitor between the gate terminals of power-switches and the output terminal of the maximum circuit, the bootstrap circuit avoids the threshold voltage drop of power-switches. Concerning the DC-DC converter designed by a 1.2 μm CMOS technology, SPICE [18] simulations are performed. In SPICE simulations, the characteristics of the proposed bootstrapped gate transfer switches are compared with that of the conventional circuit [14]. Furthermore, concerning the bootstrap circuit, experiments are performed to confirm the validity of circuit design.

2. Ring-Type DC-DC Converter

Figure 1 shows an example of ring-type power converters [1]. By controlling the power-switches $S_{i,j}$ ($(i = 1,\ldots,4)$ and $(j = 1,\ldots,3)$), the circuit converts a voltage to other by means of changing the connections of capacitors, C_j's ($j = 1,\ldots,3$). The clock pulses for $S_{i,j}$ are non-overlapped 3-phase pulses $\Phi_{i,j}$, and the clock pulses for $S_{2,j}$ are set to the inverted pulses of $\Phi_{1,j}$. The switches $S_{3,j}$ and $S_{4,j}$ are driven by the clock pulses obtained by shifting the clock-pulses $\Phi_{1,j}$ cyclically. When the output current is 0 and the voltage-drop caused by power-switches is free, the output voltage V_{out} is given by

$$V_{out} = \frac{Q}{P} V_{in}, \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (1)$$

* Kumamoto National College of Technology
2659-2, Suya, Nishigoshi, Kikuchi, Kumamoto, Japan 861-1102
** Hiroshima Kokusai Gakuin University
6-20-1, Nakanom Akiku, Hiroshima, Japan 739-0321
*** Sojo University
1-2-70, Nishihara, Kumamoto, Japan 862-0929
**** Kumamoto University
2-40-1, Kurokami, Kumamoto, Japan 860-8555

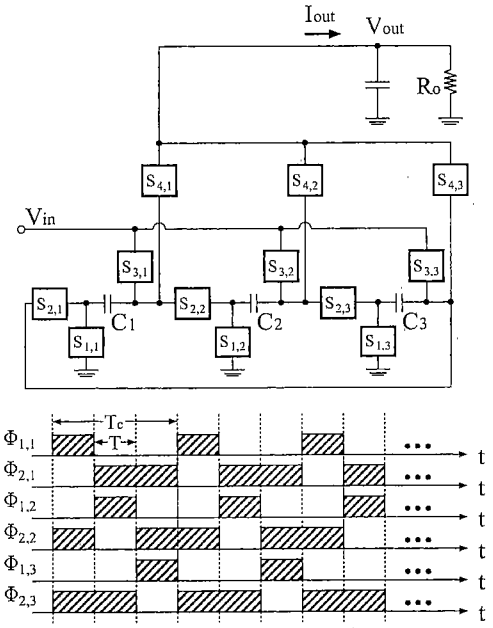


Fig. 1. Block diagram of a ring-type power converter. ($\max(V_{out}) = 3V_{in}$ and $\min(V_{out}) = V_{in}/3.$).

where

$$P \in \{1,2,3\} \quad \text{and} \quad Q \in \{1,2,3\}.$$

In Eq.(1), P and Q denote the number of the capacitors connected to the input terminal and the output terminal, respectively. The parameters P and Q are determined by the timing of the clock pulses for $S_{3,j}$ and $S_{4,j}$ $(j = 1, \ldots, 3)$, respectively. Thus the ring-type power converter works as a step-up and step-down DC-DC converter by controlling the ratio of the parameters P and Q.

3. Bootstrapped Gate Transfer Switch

3.1 Proposed Circuit SC power conversion circuits consist of only power-switches, capacitors, and clock-pulse generators. The key for the efficient design of SC converters is a design of power-switches.

Figure 2 shows a bootstrapped gate transfer switch used in the proposed power conversion circuit. In Fig.2, the inputs V_{x0} and V_{xp}'s $(p = 1, \ldots, N)$ are connected to the voltage source V_{in} and the nodes V_{xp}'s which are the right terminals of capacitors C_j's. The parameter M in Fig.2 denotes the number of the serial-connected PMOSFET's MI_k $(k = 1, \ldots, M)$. To operate the building block which is constructed with MI_l $(l = 0, \ldots, M)$ as an inverter, the parameter M is determined to satisfy

$$\sum_{k=1}^{M} R_{dk} \gg R_{d0} \ (\simeq 0) \quad (\text{if } \Phi_{\mathrm{in}} = \text{high})$$
$$\text{and} \quad \sum_{k=1}^{M} R_{dk} \ (\simeq 0) \ll R_{d0}, \quad (\text{if } \Phi_{\mathrm{in}} = \text{low}),$$

where R_{dl} denotes the drain-source resistance of MI_l.

During the input pulse Φ_{in} is high, the MOS-switches M1, M2, and M5 are *on*, and the MOS-switches M3 and M4 are off. In this timing, the capacitor C_b is charged by the maximum voltage V_{max} of V_{xq}'s $(q = 0, 1, \ldots, N)$. When voltage-drop caused by MOS-switches is 0, the capacitor C_b is charged to $V_{max} - V_{th}$, where V_{th} denotes the threshold voltage of diodes.

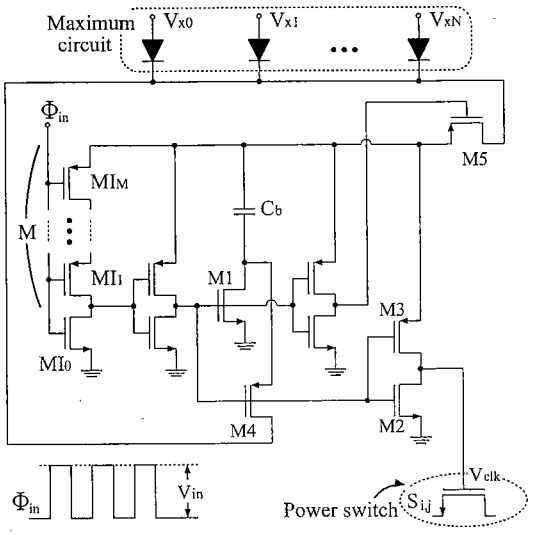


Fig. 2. Proposed bootstrapped gate transfer switch.

On the other hand, during Φ_{in} is low, the states of MOS-switches M1, M2, M3, M4, and M5 are reversed. Via M3, C_b, and M4, the gate terminal of the power-switch $S_{i,j}$ is driven by the output voltage V_{clk}. When voltage-drop caused by MOS-switches is 0, the output voltage V_{clk} is given by

$$V_{clk} = \begin{cases} 2(V_{max} - V_{th}) & \text{if} \quad \Phi_{\mathrm{in}} = \text{low}, \\ 0 & \text{if} \quad \Phi_{\mathrm{in}} = \text{high}, \end{cases} \quad \cdots (2)$$

where

$$V_{max} = \max\{V_{x0}, V_{x1}, \ldots, V_{xN}\}.$$

In Fig.2, the output voltages V_{clk} and $\overline{V_{clk}}$ are used as the clock pulses $\Phi_{1,j}$ (or $\Phi_{3,j}$ or $\Phi_{4,j}$) and $\Phi_{2,j}$, respectively.

3.2 Conventional Circuit Figure 3 shows the conventional bootstrapped gate transfer switch proposed in [14] †. In this circuit, the output pulse V_{clk} is given by

$$V_{clk} = \begin{cases} V_y + V_{in} & \text{if} \quad \Phi_{\mathrm{i,j}} = \text{low}, \\ 0 & \text{if} \quad \Phi_{\mathrm{i,j}} = \text{high}, \end{cases} \quad \cdots\cdots (3)$$

where V_y denotes a source voltage of a power-switch. As Eq.(3) shows, the conventional circuits are connected to all the power-switches in the power converter.

3.3 Comparison Since V_y in Eq.(3) satisfies $V_{max} \geq V_y$, the maximum value of V_{clk} for the conventional circuit, $\max(V_{clk})$, is given by

$$\max(V_{clk}) = \begin{cases} V_{max} + V_{in} & \text{if} \quad \Phi_{\mathrm{i,j}} = \text{low}, \\ 0 & \text{if} \quad \Phi_{\mathrm{i,j}} = \text{high}. \end{cases}$$
$$\cdots\cdots\cdots\cdots\cdots\cdots (4)$$

From Eqs.(2) and (4), the amplitude of the output voltages for these bootstrap circuits is given as shown in

† Of course, several types of power converters have been proposed [15]~[17]. Among others, Myono et al. proposed efficient circuits by employing level shift circuits [16]. However, these circuits cannot be adopted to step-up and step-down power converters such as ring-type power converters, cell-network type power converters, etc..

Fig.4. In Fig.4, we assume that the power conversion circuits are used for mobile equipments †. The threshold voltage of diode, V_{th}, and input voltage V_{in} were set to $0.6V$ and $3.5V$, respectively. In a step-down process, the output voltage of the proposed bootstrap circuit is smaller than that of the conventional circuit. However, the gate terminals of power-switches can be driven by higher voltages than that of the source terminals since the source voltages of power-switches are smaller than V_{in} (see in Fig.4). Furthermore, Eq.(2) can be rewritten as

$$V_{clk} \simeq \begin{cases} 2V_{max} & \text{if } \Phi_{\text{in}} = \text{low}, \\ 0 & \text{if } \Phi_{\text{in}} = \text{high}, \end{cases} \quad \cdots\cdots\cdots (5)$$

when the input voltage satisfies $V_{in} \gg V_{th}$. Hence, in spite of a step-down process, the output voltage of the proposed bootstrap circuit approaches to that of the conventional circuit when $V_{in} \gg V_{th}$.

For a proposed bootstrap circuit, $12+M$ MOSFET's, $N+1$ diodes, and a capacitor are required. On the other hand, 11 MOSFET's and 3 capacitors are required for a conventional bootstrap circuit. In point of the number of elements, the number of MOSFET's for the conventional circuit is less than that for the proposed circuit. However, the number of capacitors for the conventional circuit is larger than that for the proposed circuit. Generally speaking, the size of capacitors is quite larger than that of MOSFET's. Furthermore, the number of the conventional bootstrap circuits is larger than that of the proposed bootstrap circuits. The number of the conventional circuits is equal to that of power-switches since the input terminal V_y must be connected to each source terminal of power-switches [14]. For example, in case of the circuit shown in Fig.1, 12 bootstrap circuits are required. In the proposed circuit, there is no need to connect the bootstrap circuits to each source terminal of power-switches. The power-switches $S_{1,j}$, $S_{3,j}$, and $S_{4,j}$ are driven by the same voltage V_{clk}. Therefore, the number of the bootstrap circuits is double for that of the phases of $\Phi_{i,j}$. For example, in case of the circuit shown in Fig.1, the number of the bootstrap circuits is 6.

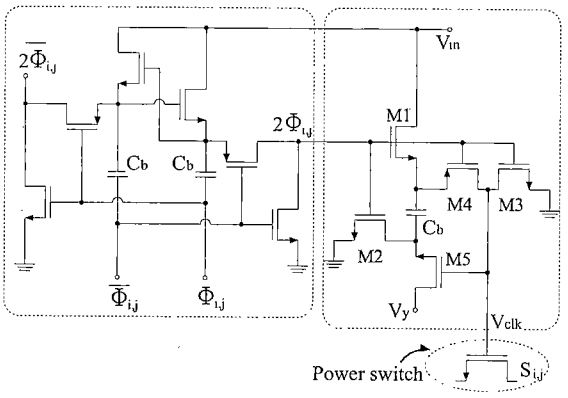


Fig. 3. Conventional bootstrapped gate transfer switch.

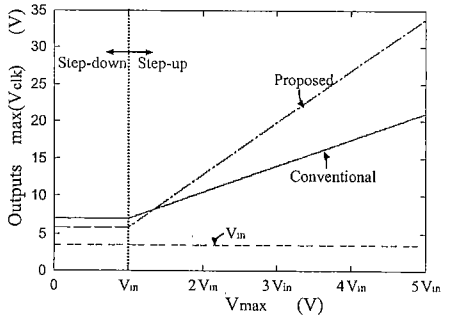


Fig. 4. Comparison of the output voltages of the bootstrap circuits.

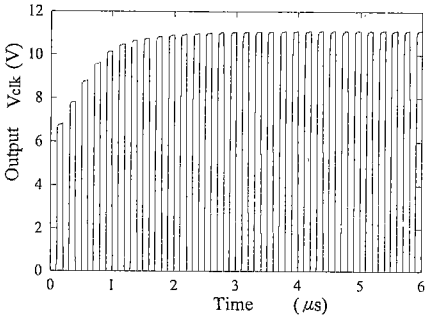
† The voltage of the lithium battery used in the mobile equipments is about $2.8 \sim 3.8$ V.

4. Simulation

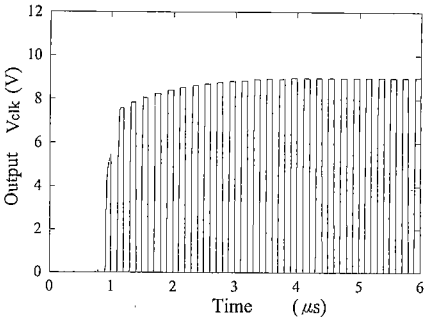
To confirm the validity of circuit design, SPICE simulations were performed concerning the circuits which were designed by assuming a 1.2 μm process produced by On-Semiconductor.

Figure 5 shows the simulated characteristics of bootstrap circuits. Figure 5 (a) shows the simulated characteristics of the proposed circuit shown in Fig.2. Figure 5 (b) shows the simulated characteristics of the conventional circuit shown in Fig.3. In Fig.5, the amplitude of input pulse Φ_{in} and the supply voltage V_{in} were set to $3V$. The source voltage of power-switches and the nodes V_{xi}'s were set to $6V$. As Fig.5 shows, the amplitude of output pulse V_{clk} for the proposed circuit is larger than that of the conventional circuit proposed in [14]. In other word, small on-resistance can be realized by using the proposed circuit.

Figure 6 shows the simulated outputs of Fig.1 with

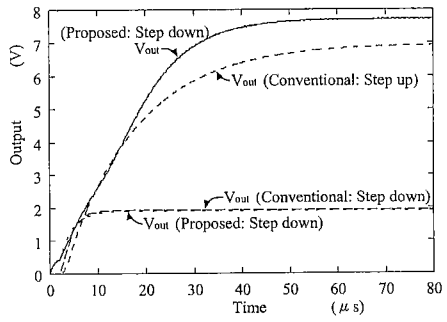


(a) Proposed.

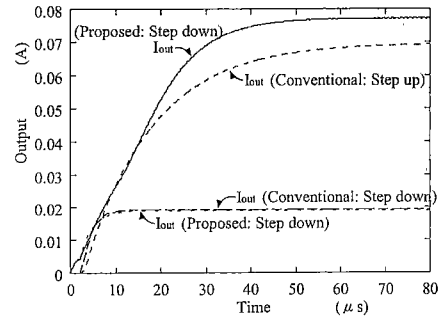


(b) Conventional.

Fig. 5. Simulated characteristics of bootstrap circuits.

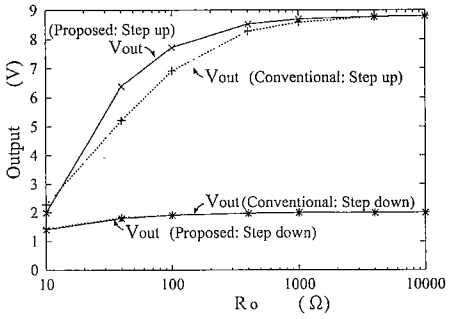


(a) Output voltages.

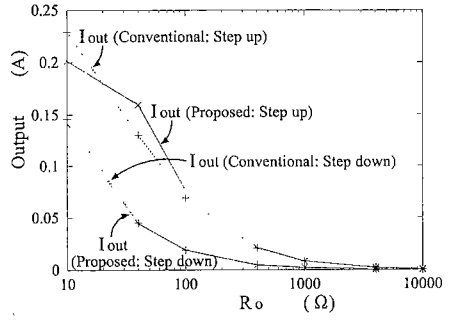


(b) Output currents.

Fig. 6. Simulated outputs of the power converter when $R_o = 100\Omega$.



(a) Output voltages.



(b) Output currents.

Fig. 7. Simulated outputs for the output load R_o.

Table 1. Timing of the clock pulses in case of $3V_{in}$.

	Clock pulse			On timing $(n = 1, 2, 3, \ldots)$
1	$\Phi_{1,1}$	for	$S_{1,1}$	$3n$
2	$\Phi_{1,2}$	for	$S_{1,2}$	$3n+1$
3	$\Phi_{1,3}$	for	$S_{1,3}$	$3n+2$
4	$\Phi_{2,1}$	for	$S_{2,1}$	$3n+1,\ 3n+2$
5	$\Phi_{2,2}$	for	$S_{2,2}$	$3n+2,\ 3n$
6	$\Phi_{2,3}$	for	$S_{2,3}$	$3n,\ 3n+1$
7	$\Phi_{3,1}$	for	$S_{3,1}$	$3n$
8	$\Phi_{3,2}$	for	$S_{3,2}$	$3n+1$
9	$\Phi_{3,3}$	for	$S_{3,3}$	$3n+2$
10	$\Phi_{4,1}$	for	$S_{4,1}$	$3n+1$
11	$\Phi_{4,2}$	for	$S_{4,2}$	$3n+2$
12	$\Phi_{4,3}$	for	$S_{4,3}$	$3n$

Table 2. Timing of the clock pulses in case of $2V_{in}/3$.

	Clock pulse			On timing $(n = 1, 2, 3, \ldots)$
1	$\Phi_{1,1}$	for	$S_{1,1}$	$3n$
2	$\Phi_{1,2}$	for	$S_{1,2}$	$3n+1$
3	$\Phi_{1,3}$	for	$S_{1,3}$	$3n+2$
4	$\Phi_{2,1}$	for	$S_{2,1}$	$3n+1,\ 3n+2$
5	$\Phi_{2,2}$	for	$S_{2,2}$	$3n+2,\ 3n$
6	$\Phi_{2,3}$	for	$S_{2,3}$	$3n,\ 3n+1$
7	$\Phi_{3,1}$	for	$S_{3,1}$	$3n+1$
8	$\Phi_{3,2}$	for	$S_{3,2}$	$3n+2$
9	$\Phi_{3,3}$	for	$S_{3,3}$	$3n$
10	$\Phi_{4,1}$	for	$S_{4,1}$	$3n+2$
11	$\Phi_{4,2}$	for	$S_{4,2}$	$3n$
12	$\Phi_{4,3}$	for	$S_{4,3}$	$3n+1$

bootstrap circuits. The circuits for Figs.6 (a) and (b) were constructed by using the proposed bootstrap circuit shown in Fig.2 and the conventional bootstrap circuit shown in Fig.3, respectively. The proposed bootstrap circuits used in the simulated converter consist of 126 (= 21 × 6) † MOSFET's and 6 (= 1 × 6) capacitors. On the other hand, the conventional bootstrap circuits used in the simulated converter consist of 132 (= 11 × 12) MOSFET's and 36 (= 3 × 12) capacitors. In Fig.1, the power-switches were constructed with parallel-connected MOSFET's. The SPICE simulations were performed under the conditions that $V_{in} = 3V$, $C_j = 500nF$, $C_b = 1nF$, $R_o = 100\Omega$, $T = 1\mu s$, and on-resistance of the power-switch, $R_{on} = 1.8\Omega$. To obtain $3V_{in}$ and $2V_{in}/3$ as the output voltages, the timing of the clock pulses was set to as shown in Tables 1 and 2. The *ideal* voltages for the step-up/step-down outputs, $3V_{in}$ and $2V_{in}/3$, are $9V$ and $2V$, respectively. As Fig.6 shows, the proposed circuit can achieve efficient DC-DC conversion. The proposed circuit improved efficiency up to 8.7 % of a conventional converter.

To investigate the effect of output load, the output characteristics were investigated by controlling R_o. Figure 7 shows the effect of output load concerning the power converters. Figure 8 shows the efficiency of the power converters for the output load R_o. In the proposed circuit, the efficiency of DC-DC conversion is more than 90 % when $R_o > 200\Omega$ ††.

5. Experiment

To confirm the validity of circuit design, the experimental circuit for Fig.2 was built with commercially available IC's, 4007UBP, 4528UBP, and capacitors. To generate the input pulse $\Phi_{\rm in}$, the 4528UBP was used in the experimental circuit.

Figure 9 shows measured output voltage of the experimental circuit. In Fig.9, the experiment was performed

† The parameter M in Fig.2 was set to 5. And the diodes in the maximum circuit were designed by using MOSFET's.

†† Of course, the efficiency of these power converters can be improved by increasing the number of parallel-connected MOSFET's in the power-switch.

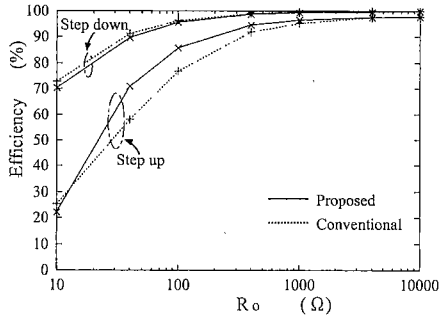
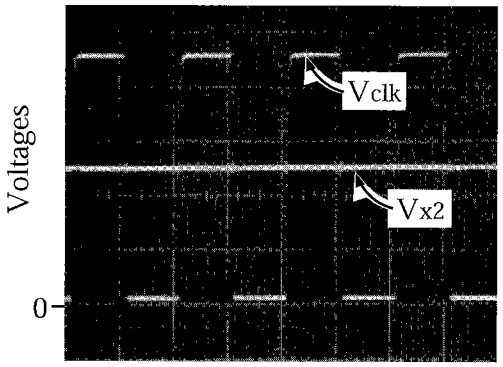


Fig. 8. Efficiency of the power converter.



Ver.: 2 V/div., Hori.: 5 μs/div.

Fig. 9. Measured output of the proposed bootstrap circuit.

under the condition that $V_{x0} = 1.0V$, $V_{x1} = 3.0V$, $V_{x2} = 5.0V$, $T_c = 10\mu s$, and $C_b = 5.1nF$ † . As Fig.9 shows, the proposed bootstrap circuit can provide a step-up voltage V_{clk}.

6. Conclusion

A ring-type SC DC-DC converter with bootstrapped gate transfer switches has been proposed in this paper. The SPICE simulations and experiments showed the following results: 1. The efficiency of the proposed power converter was more than 90 % when the output load satisfies $R_o > 200\Omega$. When $R_o = 100\Omega$, the circuit improved efficiency up to 8.7 % of a conventional converter. 2. The size of the proposed converter is smaller than that of the conventional converter. In case of the simulated circuits, 126 MOSFET's and 6 capacitors were required in the proposed circuit. On the other hand, 132 MOSFET's and 36 capacitors were required in the conventional circuit. 3. The experiments for a breadboard circuit showed the validity of the circuit design.

An IC integration of the power converter with the proposed bootstrap circuits is left to the future study.

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† Since the characteristics of discrete elements used in the experimental circuit are quite different from that of the elements used in the SPICE simulations, we chose above-mentioned setting.

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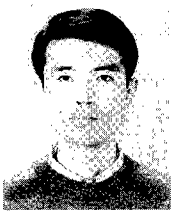
Kei Eguchi (Member) received the B.E., the M.E., and the D.E. degrees from Kumamoto University, Kumamoto, Japan in 1994, 1996, and 1999, respectively. Presently he is an Associate Professor in Kumamoto National College of Technology. His research interests include nonlinear dynamical systems, intelligent circuits and systems, and low-voltage analog integrated circuits. He is a member of IEICE.

Toru Tabata (Non-member) was born in Kumamoto, Japan in 1946. He received the B.E., the M.E., and the D.E. degree in electrical engineering from Kumamoto University, Kumamoto, Japan, in 1970, 1972, and 1999, respectively. Currently, he is a Professor of the Department of Electronic Control at Kumamoto National College of Technology. His research interests and activities include the multiple-valued computer arithmetic circuits. He is a member of IEICE and IPS of Japan.

Hongbing Zhu (Member) has the B.S., the M.S. and the the Ph.D. degrees. He was an Assistant Professor and Lecture of Information Science & Engineering faculty, Wuhan University of Science & Technology, and Information Processing Center, Kumamoto University. And he worked as a visiting scholar at Kyushu Tokai University and Kumamoto University. Now, he is an Associate Professor of Hiroshima Kokusai Gakuin University. His current research interests include neural networks, non Neumann computer and high-speed processing, etc.. He is also a member of IEEE, IEICE, JNNS, IPSJ.



Fumio Ueno (Member) received the B.E. degree in electrical engineering from Kumamoto University, Kumamoto, Japan, in 1955, and M.E. degree and D.E. degree from Kyusyu University Fukuoka, Japan, in 1964, 1968 respectively. He was the faculty of Kumamoto University, where he was a Professor, Dean in 1992. Since 1994 he has been the President at Kumamoto National College of Technology, and IEICE Kyusyu Branch Chair in 1995. His main interest lies in the field of active networks. Dr. Ueno is a member of IEICE, Japan Society for Fuzzy Theory and Systems, and IEEE.

Ichirou Oota (Member) received the B.Eng., the M.Eng., and the D.Eng. degree in electrical engineering from Kumamoto University, Kumamoto, Japan, in 1979, 1981, and 1991, respectively. He has been with Kumamoto National College of Technology, where he is now a Professor. His research interests include switched-capacitor circuits, switching converters, and computer simulation for switching circuits.

Takahiro Inoue (Member) received the B.E. and the M.E. degree from Kumamoto University, Kumamoto, Japan in 1969 and 1971, respectively, and the D.E. degree from Kyushu University, Fukuoka, Japan in 1982. From 1971 to 1974, he worked as a Research Staff at Hitachi, Ltd., Yokohama, Japan. In 1975, he joined the faculty of Kumamoto University, where he is now a Professor. Dr. Inoue's current research interests include switched-capacitor/switched-current filters, continuous-time IC filters, low-power/low-voltage analog integrated circuits, and analog/digital intelligent circuits and systems. He is a member of the Institute of Electrical and Electronics Engineers and he served as an Associate Editor of Transactions on Fuzzy Systems during 1994-1996. He is also a member of the Japanese Neural Network Society, and the Physical Society of Japan.