Paper

Design of a Random-Switching Controller Using Chaos Generators

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In this paper, a random-switching controller using chaos generators is employed in a DC-DC converter. By fluctuating the timing of the clock pulse for the converter, the controller can reduce the peaks of the power-spectrum of the output voltage. Different from the conventional controllers, the proposed controller exploits random noise generated by chaos generators. Therefore, the proposed controller can achieve effective reduction of the noise spectrum peak with small size of circuit. Concerning the controller designed by a 1.2 μm CMOS technology, SPICE simulations are performed to investigate the characteristics of the circuit. The SPICE simulations show that 1. the noise spectrum peak of the output voltage of the power converter is reduced more than $10dB$ by employing the controller and 2. the circuit size for the proposed controller is smaller than that for the conventional controller. Furthermore, the validity of the circuit design is confirmed by experiments. The proposed controller will be applicable for most of switching power converters without design modification for the other parts.

Keywords: noise spread spectrum techniques, chaos circuits, DC-DC converters, pulse width modulation methods, discrete-time circuits, analog circuits

1. Introduction

A power converter [1]~[4] is one of the most important building blocks in the electronic equipments. Among others, the switching converters have been commonly employed. In the design of the switching converters, the effect of the switching noise is a serious problem. For this reason, to reduce the effect of the switching noise, several techniques such as filters, snubbers, etc. have been developed. However, these methods require very complex circuitry and the size of the power converter becomes large. Being distinct from such techniques, recently, random-switching control [5]~[8] attracts many researchers' attention. By spreading the noise power in frequency domain, this method can reduce electro-magnetic interference (EMI). In the realization of the random-switching controllers, the digital circuits generating pseudo random noise have been employed. For example, Sadamura et al. proposed an FPGA-implemented controller with M-sequence generator [8]. The performance of the conventional controllers using pseudo random noise depends on the bit-length of the generator. Therefore, to improve its performance, the size of the circuit becomes larger.

In this paper, a random-switching controller using chaos generators [9]~[12] is employed in a DC-DC converter. By fluctuating the timing of the clock pulse for the converter, the controller can reduce the peaks of the power-spectrum of the converter. Different from the conventional controllers, the proposed controller exploits random noise generated by chaos generators. Therefore, the controller can achieve effective reduction of the noise spectrum peak with small size of circuit. Concerning the controller designed by a 1.2 μm CMOS technology, SPICE simulations are performed to investigate the characteristics of the circuit. Furthermore, to confirm the validity of the circuit design, experiments are performed concerning the experimental circuit which is built with commercially available IC's.

2. Circuit Structure

Figure 1 shows an architecture of the power converter with the proposed random-switching controller. The system shown in Fig.1 consists of a chaos generator, a clock pulse generator, and a power converter. In Fig.1, $X_i(0)$'s and $C_i(t)$'s $(i = 1, 2, \ldots, M)$ denote initial values for the chaos generator and chaos signals of the chaos generator, respectively. The switches of the power converter are driven by the modulated clock pulses which are generated by the proposed controller. In the power

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converter, the input voltage V_{in} is converted to V_{out}. As Fig.1 shows, the proposed controller can be applied for most of switching power converters without design modification for the other parts.

Figure 2 shows an example of the chaos generators designed by using a switched-current (SI) technique [12]. The circuit of Fig.2 is a 1-dimensional chaos generator realizing a tent map. The circuit operates the following equation:

$$C_i(t) \triangleq \begin{cases} 1 & (\mathrm{X}_i(t) > 0.5), \\ 0 & (\mathrm{X}_i(t) \le 0.5), \end{cases} \quad \cdots\cdots (1)$$

where

$$\begin{aligned} \mathrm{X}_i(t+1) &= \mathrm{F}(\mathrm{X}_i(t)) \\ &= 2\{\mathrm{X}_i(t) \ominus 2(\mathrm{X}_i(t) \ominus 0.5)\}. \quad \cdots\cdots (2) \end{aligned}$$

In Eq.(2), the symbol $\ominus$ denotes a bounded difference operator defined by

$$\alpha \ominus \beta \triangleq \begin{cases} \alpha - \beta & \text{if} \quad \alpha > \beta, \\ 0 & \text{if} \quad \alpha \le \beta. \end{cases}$$

The nonlinear function $\mathrm{F}(\cdot)$ in Eq.(2) is realized by the bounded difference circuit in Fig.2. The output of the bounded difference circuit is delayed by one clock in the SI track & hold circuit. In Fig.2, the current sources I_1 and I_b are set to the values corresponding to 0.5 in Eqs.(2) and (1), respectively.

Figure 3 shows the clock pulse generator used in the proposed controller. In this figure, $C_i(t)$'s $(i = 1, 2, \ldots, M)$ denote the random signals which are given by the chaos generator. The frequency of the oscillation, f_p, is determined to satisfy

$$f_c \neq q f_p \ (q = 1, 2, 3, \ldots) \ \text{and} \ \frac{f_c}{f_p} > 1, \quad \cdots\cdots (3)$$

where f_c $(= 1/T)$ denotes the frequency of the chaos generator. The operation of this circuit is as follows.

• Initial state:

In the initial condition, the node b is in *high* state if the node a is in *low* state. Then the capacitor C_c is charged by the power supply V_{dd} via MOSFET $M1$. In this timing, the circuit in Fig.3 can be expressed by the equivalent circuit shown in Fig.4 when we assume that the voltage-drop caused by MOSFET's is 0. Since the circuit of Fig.4 is a series connected circuit which consists of C_c and $R_c + \sum_{i=1}^{M} Rs_i\overline{C_i(t)}$, the speed of the charging to C_c is determined by the time constant

$$\tau = C_c(R_c + \sum_{i=1}^{M} Rs_i\overline{C_i(t)}).$$

In other word, the speed of the charging depends on the chaos signal $C_i(t)$. For example, the frequency of the oscillation becomes faster when the number of the *on*-state

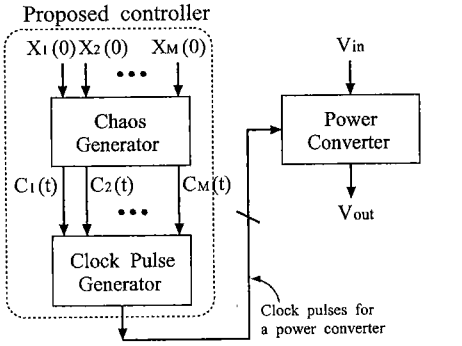


Fig. 1. Architecture of a power converter with the proposed random-switching controller.

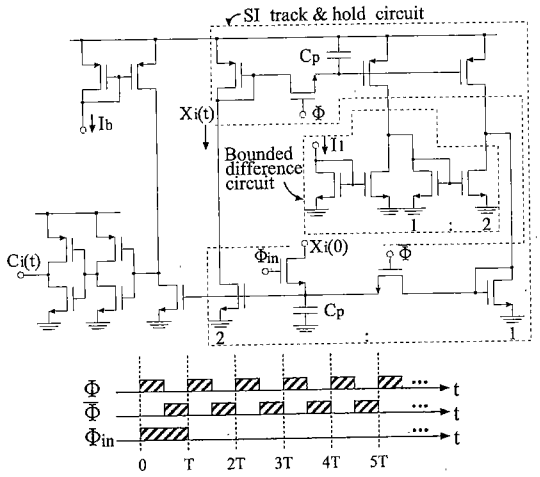


Fig. 2. An example of the chaos generators.

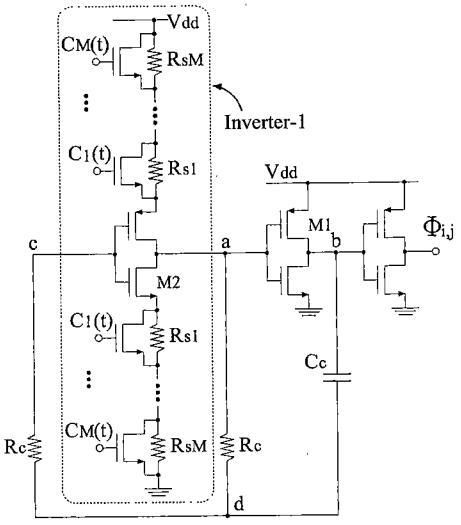


Fig. 3. Clock pulse generator.

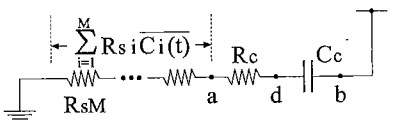


Fig. 4. Equivalent circuit of Fig.3 when the states of the nodes a, b, and c are *low*, *high*, and *high*, respectively.

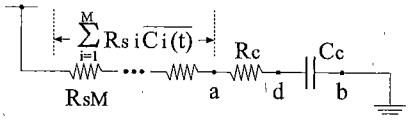


Fig. 5. Equivalent circuit of Fig.3 when the states of the nodes a, b, and c are *high*, *low*, and *low*, respectively.

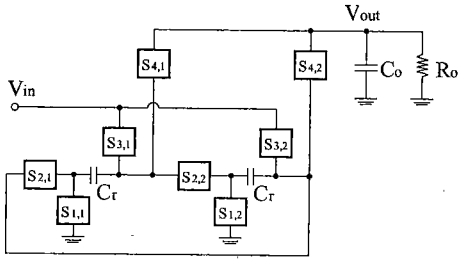


Fig. 6. Power converter used in the SPICE simulations.

$C_i(t)$ is increasing [†] .

- **State-I:**

When the charging to the capacitor C_c starts, the state of the node c is *high*. However, the voltage of the node c decreases according to the time of the charging. In the long run, the voltage of the node c becomes lower than the threshold voltage of the inverter-1. In this timing, the states of the nodes a, b, and c are reversed. From Eq.(3), the reverse of the state has two cases: 1. the states of $C_i(t)$'s are not changed during C_c is charging and 2. the states of $C_i(t)$'s are changed during C_c is charging. In the latter case, the frequency of the oscillation is changed by the states of $C_i(t)$'s according to the value of $\sum_{i=1}^{M} Rs_i\overline{C_i(t)}$.

- **State-II:**

The circuit in Fig.3 can be expressed by the equivalent circuit shown in Fig.5 since the states a, b, and c of the nodes are *high*, *low*, and *low*, respectively. In this timing, the discharging from capacitor C_c starts. Then, the voltage of the node c increases according to the time of the discharging. In the long run, the voltage of the node c becomes higher than the threshold voltage of the inverter-1. In this timing, the states of the nodes a, b, and c are turned into *low*, *high*, and *high*, respectively. As in the case of *State*-I, the frequency of the oscillation depends on the frequency f_c and the states of $C_i(t)$'s.

The modulation of the clock pulse is performed by reiterating *State*-I and *State*-II, alternately.

[†]When on-resistance R_{oni} of series-connected MOSFET in the inverter-1 doesn't satisfy $R_{oni} \ll Rs_i$, the time constant is given by

$$\tau = C_c(R_c + \sum_{i=1}^{M} Z_i(t)),$$

$$Z_i(t) \triangleq \begin{cases} \dfrac{Rs_i R_{oni}}{Rs_i + R_{oni}} & \text{if} \quad C_i(t) = 1, \\ Rs_i & \text{if} \quad C_i(t) = 0. \end{cases}$$

Hence the frequency of the oscillation changes from above-mentioned case.

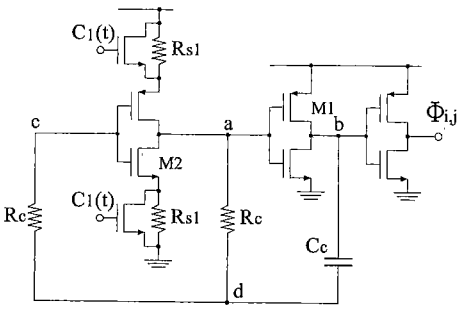


Fig. 7. Clock pulse generator used in the SPICE simulations.

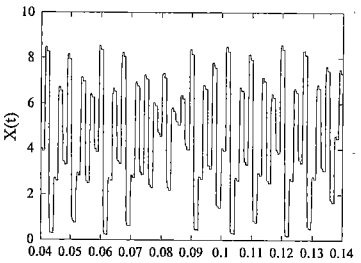


Fig. 8. An example of the chaotic signals.

3. Simulation

To confirm the validity of circuit design, SPICE simulations were performed concerning the proposed controller designed by assuming a 1.2 μm CMOS process. In the simulations, the switched-capacitor (SC) power converter of Fig.6 [(3)] was used as the power converter shown in Fig.1. By controlling the power switches $S_{i,j}$ $((i = 1, 2)$ and $(j = 1, \ldots, 4))$, the circuit converts an input voltage V_{in} to

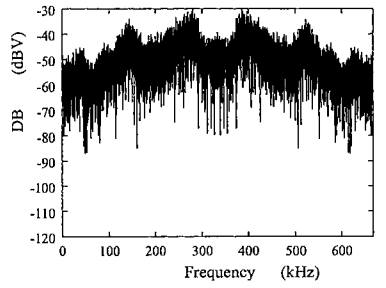
$$V_{out} = \frac{Q}{P} V_{in}, \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (4)$$

where $Q \in \{1, 2\}$ and $P \in \{1, 2\}$. The simulations were performed under the conditions that $P = 1$, $Q = 2$, $V_{in} = 3V$, $C_r = 200nF$, and $C_o = 0$ [††] . And the circuits shown in Figs.2 and 7 were used as an chaos generator and a clock pulse generator, respectively.

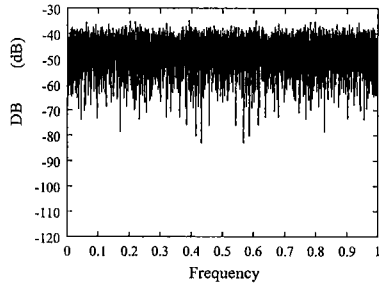
Figure 8 shows the simulated chaotic signal generated by the circuit shown in Fig.2. In Fig.8, the capacitor C_p was set to $0.6pF$ and the clock frequency was set to $2/3MHz$. Figure 9 shows the power spectrum of the circuit shown in Fig.2. Although the power spectrum of the *ideal* tent map is white spectrum, the power spectrum of Fig.2 is different from *ideal* one. As Fig.9 shows, the non-ideal effects of the circuit implementation such as the fluctuation of mobility, the variation of threshold voltage, etc. affect the characteristics of chaotic signals. To spread the noise power efficiently, the chaotic signals which have i.i.d. (independent and identically distributed) characteristics are favorable. Therefore, in the design of the chaos generator in Fig.1, the robustness of chaos signal generation is desired.

Figure 10 shows the simulated output voltage of the

[††]To stress the effect of switching noise, the capacitor C_o in Fig.6 was set to $0F$.

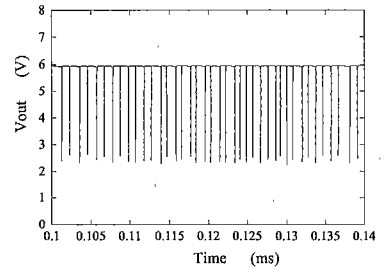


(a)

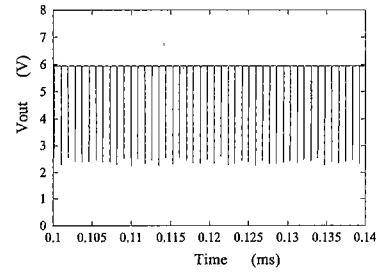


(b)

Fig. 9. Fourier spectrum of chaotic signal. (a) Chaos circuit of Fig.2. (b) *Ideal*.



(a)



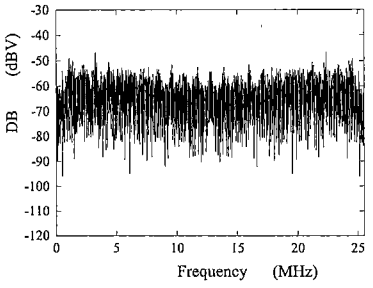
(b)

Fig. 10. Output voltage of the power converter. (a) With random-switching controller. (b) Without random-switching controller.

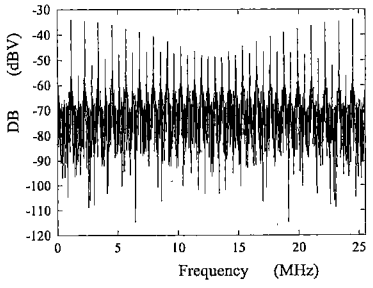
power converter. Figure 10 (a) shows the output voltage of the power converter with the proposed random-switching controller. In Fig.10 (a), the capacitor C_c, the resistors R_c and Rs_1 were set to $2pF$, 250 kΩ, and 50 kΩ, respectively. Figure 10 (b) shows the output voltage of the power converter without the proposed random-switching controller. The timing of the clock pulse $\Phi_{i,j}$ is shown in Table 1. In these figures, the ideal output voltage is 6 V. As Fig.10 shows, the pulse width modulation is achieved by the proposed controller. Figure 11 shows the power spectrum of the output voltage of the power converter. The power spectrum of Fig.11 was defined by

Table 1. Timing of the clock pulses for the power converter.

	Clock pulse	On timing $(t = 0, 1, 2, \ldots)$
1	$\Phi_{1,1}$ for $S_{1,1}$	t
2	$\Phi_{1,2}$ for $S_{1,2}$	$t+1$
3	$\Phi_{2,1}$ for $S_{2,1}$	$t+1$
4	$\Phi_{2,2}$ for $S_{2,2}$	t
5	$\Phi_{3,1}$ for $S_{3,1}$	t
6	$\Phi_{3,2}$ for $S_{3,2}$	$t+1$
7	$\Phi_{4,1}$ for $S_{4,1}$	$t+1$
8	$\Phi_{4,2}$ for $S_{4,2}$	t



(a)



(b)

Fig. 11. Fourier spectrum. (a) With random-switching controller. (b) Without random-switching controller.

$$DB = 20\log_{10}\frac{\sqrt{Re^2+Im^2}}{\max(\sqrt{Re^2+Im^2})}, \quad \cdots\cdots\cdots \quad (5)$$

$$X(k) = \sum_{n=0}^{N-1}\frac{V_{out}(n)}{\max(V_{out}(n))}e^{-j2\pi kn/N}, \quad \cdots\cdots \quad (6)$$

where

$$Re = \sum_{n=0}^{N-1}\frac{V_{out}(n)}{\max(V_{out}(n))}\cos(2\pi kn/N)$$

and $$Im = -\sum_{n=0}^{N-1}\frac{V_{out}(n)}{\max(V_{out}(n))}\sin(2\pi kn/N).$$

In Fig.11, the number of the sample, N, in Eq.(6) was set to 10,000. In Fig.11 (a), the speak around $3MHz$ is due to the non-ideal effect of the circuit implementation of the chaos circuit. As Figs.9 and 11 show, the proposed controller can reduce the noise spectrum peak in spite of the non-ideal effect of the chaos circuit. The noise spectrum peak is reduced more than $10dB$ by using the proposed controller.

To investigate the effect of random-switching for efficiency, the output characteristics of the power converters were simulated by controlling output load R_o. Figure 12

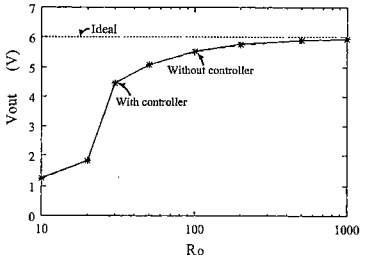


Fig. 12. Output voltage for R_o.

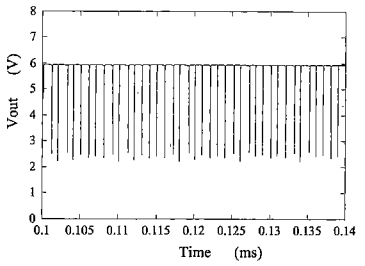


Fig. 13. Output voltage of the power converter with pseudo random-switching controller.

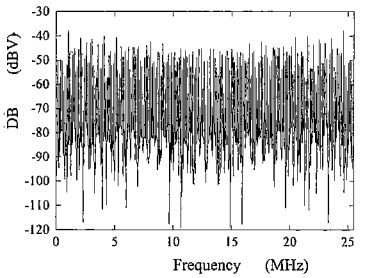


Fig. 14. Spectrum of the output voltage of the power converter with pseudo random-switching controller.

shows the output voltages † of the power converters for R_o. As Fig.12 shows, the proposed controller exerts little adverse effect on the efficiency of DC-DC conversion.

4. Discussion

Figure 13 shows the output voltage of the power converter with the pseudo random-switching controller proposed by Sadamura et al.†† [8]. In the simulation, the bit-length of the M-sequence generator was set to 3-bits. Figure 14 shows the power spectrum of the output voltage of the power converter which is obtained by using conventional controller. In Fig.14, the parameter N was also set to 10,000. As Figs.11 and 14 show, the proposed controller can achieve more effective reduction of the noise spectrum peak than the conventional

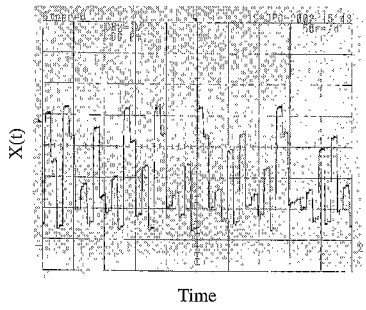


Fig. 15. Measured chaotic signal of the experimental circuit.

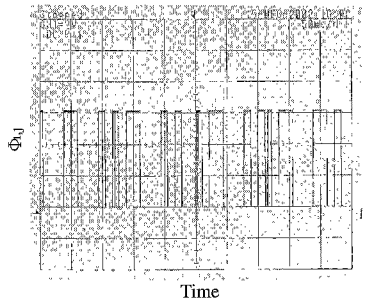


Fig. 16. Measured clock pulse generated by the random-switching controller.

controller††† . In the point of the hardware cost, the conventional circuit can be realized by about $1,680 \sim 3,360$ MOSFET's. On the other hand, the proposed controller used in the SPICE simulations requires only 27 MOSFET's, 4 resistors, and 3 capacitors. From these results, the proposed controller can achieve effective reduction of the noise spectrum peak with small size of circuit.

5. Experiment

To confirm the validity of circuit design, the experimental circuit for the proposed controller was built with commercially available IC's, 4007UB, 4528UBP, capacitors, and resistors. To generate clock pulse for the chaos generator, the 4528UBP was used in the experiments.

Figure 15 shows measured chaotic signal of the experimental circuit. Figure 16 shows measured clock pulse generated by the experimental circuit. In Figs.15 and 16, the experiment was performed under the condition that $V_{dd} = 6.0$ V, $R_c = 1500$ kΩ, $Rs_1 = 500$ kΩ, $C_c = 15$ nF, and $C_p = 10n$F. †††† . As Fig.16 shows, the experimental circuit can achieve pulse modulation.

6. Conclusion

A random-switching controller using chaos generators has been proposed in this paper. The SPICE simulations concerning the controller showed the following results. 1. By employing the proposed controller which consists of 27 MOSFET's, 4 resistors, and 3 capacitors, the noise spectrum peak of output voltage of the power converter was reduced more than $10dB$. 2. The circuit

†Of course, the efficiency of the power converters can be improved by increasing the number of parallel-connected MOSFET's in the power-switches.

††The conventional controller in [8] consists of an M-sequence generator, multiplexers, and shift-registers. According to [8], the conventional circuit can be realized by $20 \sim 40$ flip-flop circuits. In other words, the conventional circuit requires about $1,680 \sim 3,360$ MOSFET's when the flip-flop circuits are constructed with CMOS circuits.

†††Of course, the performance of the conventional controller can be improved by increasing the bit-length of the M-sequence generator. However, it takes a lot of hardware cost.

††††Since the characteristics of discrete elements used in the experimental circuit are quite different from that of the elements used in the SPICE simulations, we chose above-mentioned setting.

size for the proposed controller is smaller than that for the conventional controller.

The proposed controller can be applied for most of switching power converters without design modification for the other parts. The analyses of the effect of random-switching for switching power converters are left to the future study.

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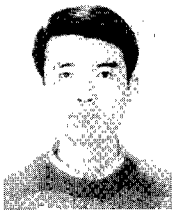

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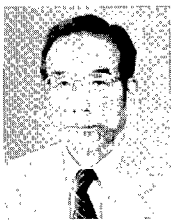

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