Paper

Optimal Thermo-Structural Analysis for High Density Package Mounting on Build-up Board

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The importance of the high density packaging technology and mounting technology on the printed wiring build-up board has been increased for the consumer electric products. On the other hand, the chance to use the build-up boards for mounting the high density packages has been increased. However, the understanding that the reliability of the solder connection depends on the structure of the package, the motherboard, and the material properties, is not very high.

In this paper, the reliability for high density packaging, mounted on the build-up board, is assessed. The compact numerical analysis model for the reliability assessment is suggested and the most reliable packaging design with optimizing each of the parameters is reported. For introduction to the reliability assessment of the FCA attachment, ceramic and silicon are compared as the inter-poser with the parameter of the solder height. The verification of the numerical analysis results using tests on the actual hardware is also shown. And the established numerical analysis model is applied to the study of influence of the copper balance between the front side and the back side copper layers.

Keywords : Fatigue, Reliability, Solder Connect, Finite Element Method, Chip Scale Package, Flip Chip Attach

1. Introduction

For the purpose of down-sizing consumer electric products, like handy phone, DVC (Digital Video Camera), DSC (Digital Still Camera), notebook PC and so on, CSP (Chip Scale Package), BGA (Ball Grid Array) and/or FCA (Flip Chip Attach) by surface mounting are becoming the important new high density packaging technology, instead of the fine pitch QFP (Quad Flat Package) mounted using perimeter leads, with being able to utilize the conventional surface mounting technology and to treat them on the same manner as the common package. They let the area of surface mounting be small. Besides, the use of build-up boards has been tried. However, the reliability of the solder connection depends on the structure of the package, the motherboard, and the material properties [(1)].

In this paper, the numerical analysis of the plastic strain with nonlinear FEM (Finite Element Method), is assessed to optimize each design parameter controlling the reliability of the connection between the package and the build-up board for the fatigue fracture by the temperature cycle stress.

On this assessment, 5 methods of the accurate and compact simulation on the view point of the reduction of the time needed for the nonlinear numerical analysis, are reported, for solder joints which are very small compared to the whole structure. And this FEM model is applied into the introduction of the FCA technology reliability assessment and the study of influence of the copper balance between the front side and the back side copper layers.

The verification of the numerical analysis results using tests on the actual hardware is also shown, and the accuracy of this numerical analysis is confirmed.

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2. Parameter Study for Build-up Board

It can be said that the build-up boards improve the design capability because they increase the wiring density by the placement of the vias on the pads for mounting the package. And, the placement of the via on the RFP (Resin Filled PTH (Pin Through Hole)) makes it easier to do the In/Out fan-out on a PWB (Printed Wiring Board). However, the more fine the pitch of the package, the more difficult it is to maintain and/or improve the reliability of the solder connection.

Especially, the difference of the coefficient of thermal expansion between the package and the build-up board, causes the large strain into the solder, and repeats the plastic displacement by the thermal cycle stress. The accumulation of this strain causes the fatigue fracture, and finally crack of the solder.

Via on RFP structure is indispensable to improve the wiring density of build-up board and mount the fine pitch package. On the other hand, the base FR4 PWB structure and the board thickness depend on the specification of the final product needs. Therefore, the specification of the board on which package is mounted, especially the part of solder connection, should be studied in detail. On this purpose, in order to obtain the most reliable design, the parameter study is performed for 6 parameters, which are thought to control that reliability, in the actually applicable range. For the introduction of the reliability assessment of the FCA technology, the plastic strain variation by the direct attachment of silicon is studied with the parameter of the solder height.

The composition shape of these parameters is shown in Figure-1. This is the cross-section figure of the part where one solder is located. The same patterns are composed side by side in this build-up board. For each parameter, the design comparison

Table 1. Parameter study.

Solder Resist Design	Over Coating				Open Window		
Copper plating thickness	4	8	15	25			
Build-up layer thickness	20	30	40	60	80		
FR4 board thickness	200	400	500	620	720	820	920
Ceramic VS Silicon	Ceramic				Silicon		
Solder Height	50 (1	50 (2	100 (2	200 (2	300 (2	400 (2	
	note : unit μm (1 : Ceramic , (2 : Silicon						

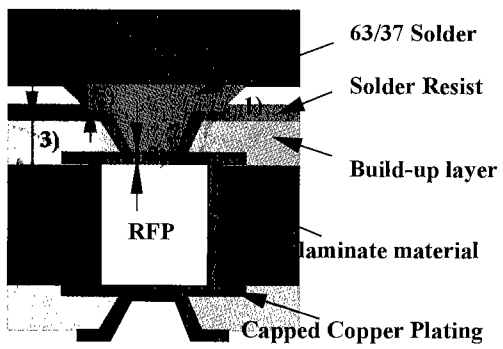

Fig. 1. Composition shape.

was performed, based on Table-1. The remaining parameters are fixed with the value of underline, when one parameter is varied.

As to Over Coating and Open Window for Solder Resist Design, the design, where Solder Resist coats the soldering pad edge and contacts the solder, means Over Coating. On the other hand, the design, where Solder Resist does not coat the soldering pad edge and there is the distance between Solder Resist and Solder, is called as Open Window.

3. Numerical Analysis

3.1 Compact Analysis Model Totally 5 compact analysis methods are applied into the FEM model to be used for analysis, shown in Figure-2. First two methods are described in this section and the remained three are done in the next 3-2 section.

Firstly, the quarter of 13mm CSP package was modeled with the detail elements for only the part where the solder receives the biggest stress, shown in Figure-2, and with the rough elements for the remains. For the rough elements, the material properties are defined with the volume ratio that covers each material. The distance between the center of a solder joint and the next one is named "one horizontal rough element unit".

The material properties to be applied for each material are given in Table-2. On the purpose of the parameter study described above, the modulus of Elasticity and the Poisson's ratio used for the ceramic and silicon are the same. The modulus of Elasticity used for solder is shown in Figure-3. As a function of temperature, this temperature dependent stress-strain curves are based on actual

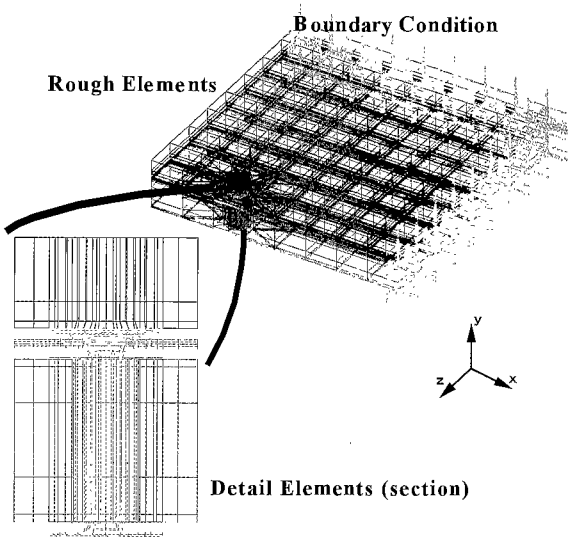

Fig. 2. Simulation model.

Table 2. Material Properties.

Material	Elasticity (Kgf/mm^2)	Poisson Ratio	Thermal Expansion Coefficient (10^{-6} 1/K)
Ceramic	3.80×10^4	0.17	6.5
Silicon	3.80×10^4	0.17	3.5
Solder	-	0.35	24.0
Solder Resist	1.84×10^2	0.25	91.0
Build-up layer	2.24×10^2	0.39	62.0
Cu plate	1.20×10^4	0.35	17.0
FR4	2.55×10^3	xy=0.3 yz=0.3 xz=0.2	x=16.0 y=55.0 z=16.0
RFP	5.84×10^2	0.30	35.0

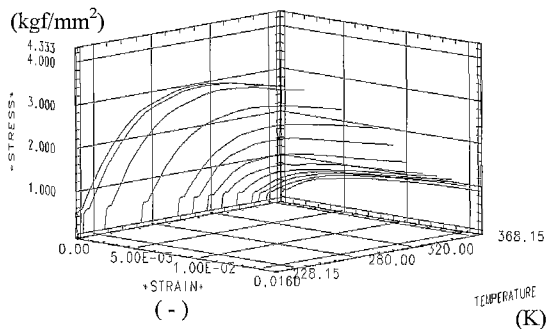

Fig. 3. Solder stress-strain curves as material property elasticity modulus.

measurements.

Secondly, the solder is located each at one horizontal rough element unit. If each solder is modeled by one horizontal rough element unit with the volume ratio method of a solder and air, the stress transfer and shear are happened among each elements. On the actual hardware, a solder displacement does not influence directly the next solder because the air exists between a solder and the next one. And this air has no restriction to move into or out

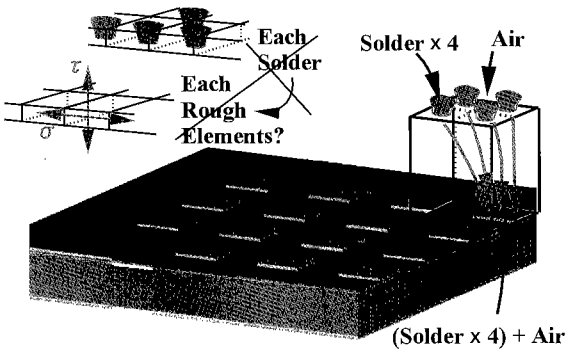

Fig. 4. Solder modeling in rough elements.

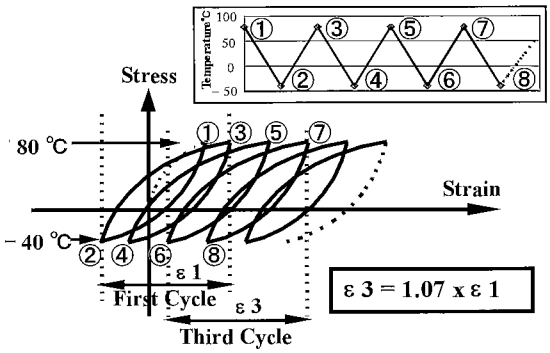

Fig. 5. Solder stress-strain curve obtained by numerical analysis (image).

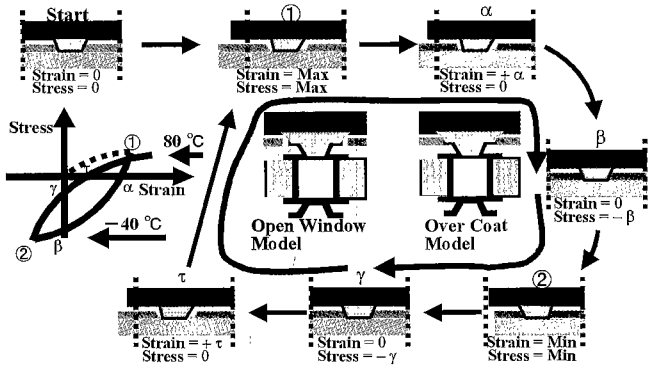

Fig. 6. Simplification of contact analysis for over coat design modeling.

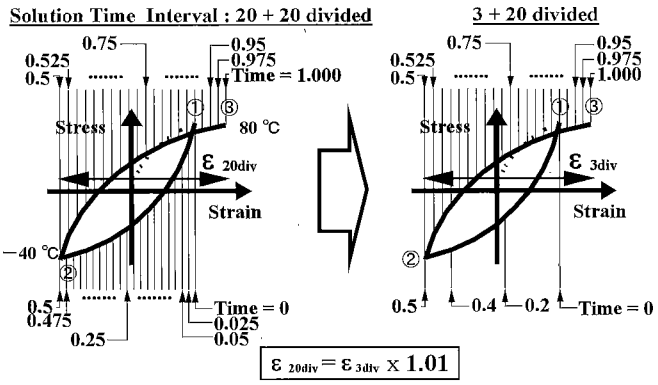

Fig. 7. Acceleration for open window design modeling.

from this CSP package. Consequently, it is difficult to simulate the actual phenomenon with this model. Therefore, in rough elements, 4 solders joints were represented by one solid rough element brick with one horizontal rough element unit, shown in Figure-4, except the solder which receives the biggest stress and/or strain. This element is surrounded by the elements that have the material property of air. With this method, the existence of air could be modeled, and besides, the merit of the rough element could be utilized.

As the boundary condition, only the bottom, in the direction of board thickness (y direction), of center of 1/4 model was clamped. Regarding the other nodes on this axis, only the y direction translation was free. As to the remained nodes located at sections, it was applied, based on the build-up board elasticity and twist toward the direction of board thickness.

3.2 Nonlinear Analysis Method Thirdly, a temperature cycle stress between 80 degree C and –40 degree C was applied. The stress-strain curve of the solder that receives the biggest stress, which got as the result by numerical analysis on this temperature cycle stress, is shown in Figure-5. The strain does not change after 2 cycles. Therefore, this value should be the accurate one to be adopted. However, it was found that this accurate value was equal to 1.07 times of the result by first cycle. Therefore, this method was taken to reduce the analysis time, to almost one third.

Fourthly, on the other hand, as to Over Coat model regarding Solder Resist, the solder receives the stress during the temperature reduction from 80 degree C to –40 degree C. However, during the rise from –40 degree C, the Solder Resist does not pull the solder because a gap is created between them. On this portion, the accurate solder strain of Over Coat design was obtained with the result by the simulation with Over Coat modeling during the temperature reduction step, and with Open Window modeling during the temperature rise step, shown in Figure-6. With this method, it was able to get the result without the long simulation time of contact analysis using gap element.

Fifthly, to obtain the value of accurate strain in the numerical simulation, the temperature cycle step should be divided at least 20 for one way, shown in Figure-7. This is called Solution Time Interval, time 0 to 1. Time 0 means analysis beginning point 80 degree C. Time 0.5 means –40 degree C. And Time 1 means returning 80 degree C. One cycle is ended. Here, the value, which is needed, is the strain that is created by the temperature increase from –40 to 80 degree C. The numerical calculation process from –40 to 80 degree C should be divided 20. However, on the first way, from 80 to –40 degree C, it is found that 20 divisions are not necessary. Therefore, Time 0.2 and 0.4 are remained, and the others are removed from the numerical calculation process. Using this method, the accurate stain was obtained around half calculation time, on the result that the strain is equal to the 20 plus 20 division's result with 1.01 times.

4. Reliability Assessment

It was defined as the metal fatigue fracture by temperature cycle stress because the typical striation was observed with the verification of the solder crack cross section that reached the fatigue fracture, shown in Figure-8. For the metal fatigue fracture

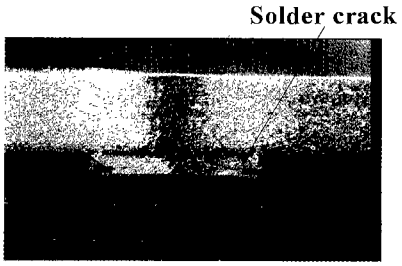

Fig. 8. Solder crack.

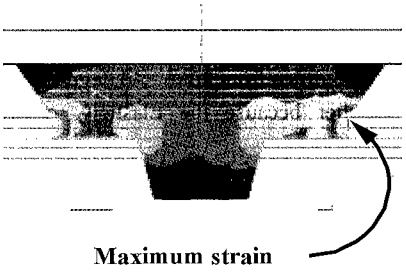

Fig. 9. Solder strain obtained by numerical simulation.

on low cycle, Coffin-Manson's reliability assessment equation is commonly used [(2)(3)].

$$Nf = C\,(\varepsilon)^{-n}$$

Where, Nf means the cycle quantity to reach the fatigue fracture, C means that metal's unique constant, ε means the plastic strain to be taken by one cycle, n means the constant, generally about 2, that means the relationship between the plastic strain and the reliability. The relative reliability assessment becomes available with the estimation of this ε by the nonlinear simulation.

Figure-9 shows the strain of the solder, obtained by the numerical analysis. It shows that the numerical simulation closely matches the actual hardware testing result.

The Coffin-Manson's equation's n is obtained as 2.05 when this simulation model is used. And C is obtained as 0.82 with some strain's data by numerical analysis and the N_{50} cumulative fracture cycles obtained by the actual hardware testing.

Finally, the reliability assessment equation on the fatigue fracture for the solder is able to be shown as the following.

$$Nf = 0.82\,(\varepsilon)^{-2.05}$$

5. Design Optimization for Best Reliability

5.1 Solder Resist Design Open Window shows twice estimated life or more, than Over Coat design with the solder strain data 2.28 versus 3.27%.

5.2 Capped Copper Plating Thickness on RFP The numerical analysis result is shown in Figure-10. The almost directly proportion relationship between the Capped Copper plating thickness on RFP and solder strain quantity is observed. However, 4 μm thickness is difficult to manufacture. Therefore, it is best to use the 8 μm thickness as of today.

Increasing the Capped Copper plating thickness on RFP means increasing the hardness of the build-up board. This also makes the bend capability of the build-up board low. The board extends more linearly than before. Because the solder is located between the ceramic, which is much harder than that, and the build-up board, as the sandwich structure, the solder has much bigger stress by the linear extension of the build-up board. It is thought that this is the reason why the solder strain increases, increasing the Capped Copper plating thickness on RFP.

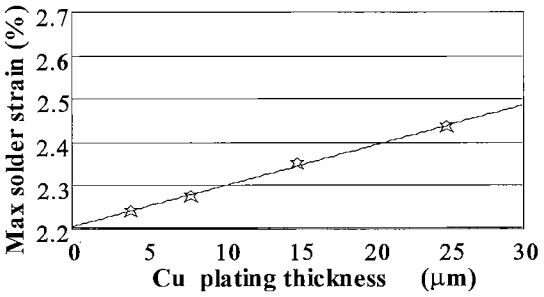

Fig. 10. Solder strain by Cu plating thickness.

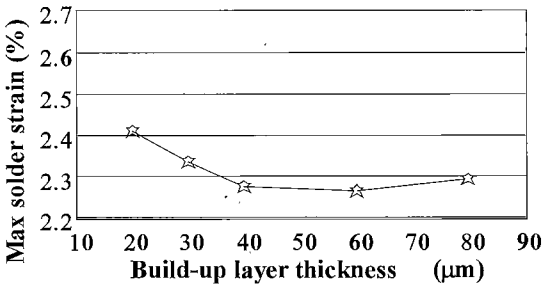

Fig. 11. Solder strain by Build-up layer thickness.

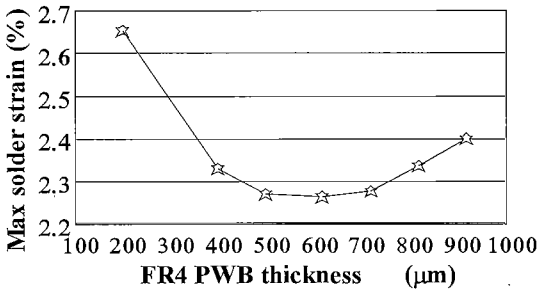

Fig. 12. Solder strain by FR4 PWB thickness.

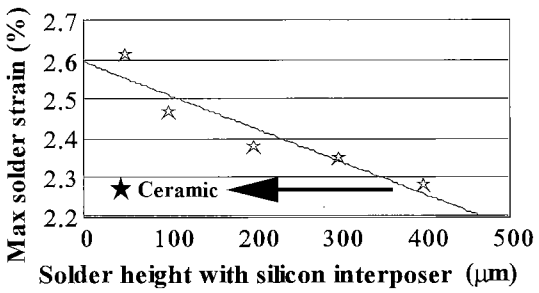

Fig. 13. Solder strain by solder height.

5.3 Build-up Layer Thickness The numerical analysis result is shown in Figure-11. When the build-up layer thickness is under 60 μm, the bigger build-up layer thickness models show the smaller strains. However, after exceeding 60 μm, the solder strain changes to the increase. Increasing build-up layer thickness means reducing the hardness as the whole board. It is thought that the opposite phenomenon happened, compared to increasing the Capped Copper plating thickness.

On the other hand, it is thought the reason why the strain is

bigger after 60 μm, is that, the height of the solder portion is increased where the diameter is smallest near the Capped Copper plating. Increasing that height, the bigger stress is taken into the solder's waist by the expansion/shrink of the board.

5.4 Base FR4 PWB Thickness The numerical analysis result is shown in Figure-12. When the base FR4 PWB thickness is over 620 μm, the bigger base FR4 PWB thickness models show the bigger strains. However, less than 620 μm, the solder strain curve has negative slope. Increasing the base FR4 PWB thickness means increasing the hardness as the whole build-up board.

This also makes the bend capability of the build-up board low. The build-up board extends more linearly than before, as the same phenomenon as 5-2. It is thought that this is also the reason why the solder strain increases, increasing the base FR4 PWB thickness.

On the other hand, it is thought the reason why the strain is bigger under 500 μm, is that the hardness for the bend is weakened too much and the ceramic restriction let the board bend much bigger. Reducing base FR4 PWB thickness under 500 μm, the bigger stress is taken into the solder's waist by the expansion/shrink of the build-up board.

5.5 Ceramic VS Silicon as the interposer For the approach toward FCA, the condition that the silicon is applied into the interposer portion, instead of ceramic, was analyzed. The simulation results yielded 2.28 % for ceramic and 2.61 % for silicon. By the just difference between ceramic and silicon, it is thought that the estimated life is reduced about 500 cycles.

5.6 Solder Height The numerical analysis result is shown in Figure-13. To approach the ceramic strain level with silicon direct mounting, it is thought that 8 times height of the solder brings the same reliability level of the solder connection, comparing to the ceramic CSP mounting. On the actual hardware, 8 times solder height of the CSP package is not applied into the FCA packaging, but approximately 2 times height is applied as the design of 100 μm with one forth solder bump pitch (200 μm) against CSP.

On the actual hardware, basically the molding encapsulant is filled between the package and the board (substrate) to help the solder enduring the stress. However, the filling of encapsulant is meaning the remarkable decrease of the rework capability. If the equivalent reliability is evaluated without encapsulant, it is useful on the view point of this capability. In approaching of the fine pitch with FCA package, decreasing the size of the build-up board mounting the package might have the possibility that the stress, which the solder receives, is decreased. On the other hand, it is also thought that the solder itself is getting much smaller, and the stress, which the solder receives from silicon that has about half coefficient of the thermal expansion of ceramic, might be increased. On these view points, the solder connection reliability assessment for FCA package needs the analysis of the circumspect and thoroughgoing approach.

5.7 Design Optimization With the analysis results stated above, if the Via on RFP structure is applied for higher density packaging, it is obtained that the most reliable design on the viewpoint of the solder connectivity reliability is as follows.

Solder Resist Design	:	Open Window
Cu plating thickness	:	8 μm
Build-up layer thickness	:	60 μm
Base FR4 PWB thickness	:	620 μm

With this design, it is obtained that the solder strain is 2.21 %. Using the Coffin-Manson's equation, the estimated life is 2051 cycles. Comparing the condition where the build-up layer thickness is 40 μm and the FR4 board thickness is 720 μm (these were original design.), 100 cycles or more extension are expected as the package products on the 80/–40 temperature cycles stress.

On the extension/shrink phenomenon of the whole build-up board mounted the package, the smaller Elasticity of the board brings the bigger displacement in y direction by the bend of the build-up board. As that result, the solder, which is located between the interposer and the build-up board, receives the smaller stress. Therefore the strain is smaller. On the condition that the temperature is going down from 80 to –40 degree C, this influence is becoming smaller because the Elasticity of the solder is increasing.

It is thought that the attempt, which reduces the Elasticity of the build-up board, contributes so much to extend the reliability of the solder connectivity, as well as, the attempt that makes the Thermal Expansion Coefficient of interposer and build-up board close.

6. Copper Balance

A build-up board (different one from stated above) has had the problem of the warpage before mounting the package on this board. The FEM model, which was established above, is applied to evaluate the warpage.

The board size is 37.5 mm square and the copper layers are totally 6. 3 out of 6 copper layers are located at front side and the remains are at back side. The cross-section of this board is shown in Figure-14. In the numerical simulation, because the variation of the copper remained ratio at edge is bigger than it at the center, the element of the edge is set to the smaller size than the center. The actual copper remained ratio is calculated for the material properties. As the sample, the copper remained ratio of the outermost front side copper layer (FC2) is shown in Figure-15.

The simulation result of this original design shows the 0.042 % as the warpage of this board with the thermal stress from 120 degree C to the room temperature 25 degree C. The problem is caused by the copper remained ratio unbalance between the front

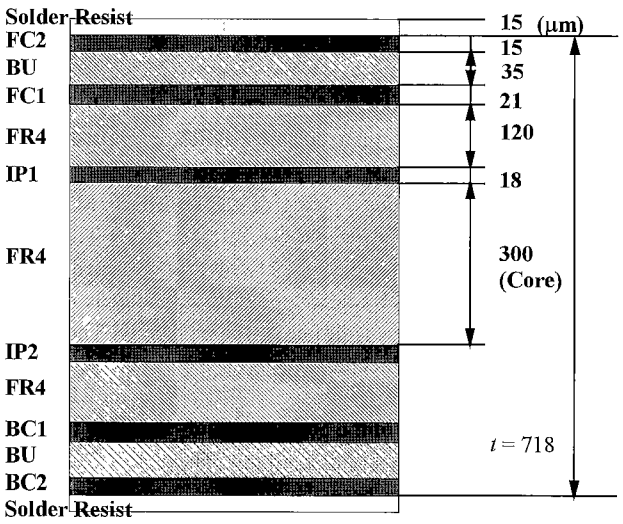

Fig. 14. Cross-section for copper balance analysis.

2.75 4.0 (mm)

61.9	63.9	77.2	77.8	72.8	72.1	70.0	67.8	70.5	42.1
65.6	57.9	88.7	98.0	68.7	60.5	37.5	37.8	31.3	45.7
71.4	33.8	26.5	81.3	28.4	28.9	25.2	22.9	58.2	69.9
69.5	32.8	22.4	29.6	40.4	30.8	33.0	26.5	43.6	72.0
71.7	43.3	14.9	31.8	49.8	50.3	30.6	34.8	46.5	64.6
68.7	41.2	16.3	30.9	47.2	45.0	31.3	26.8	39.3	70.7
71.6	43.7	22.5	35.7	33.4	31.7	29.5	24.4	37.8	71.0
68.8	38.6	22.8	23.2	20.1	21.0	23.2	20.0	43.1	71.7
52.2	46.1	28.4	20.5	21.6	23.5	55.7	38.5	27.4	60.2
56.2	63.0	70.0	70.2	66.8	71.0	70.0	70.1	69.3	41.9

(unit : %)

Fig. 15. Actual copper remained ratio of the outermost front side copper layer (FC2).

side and back side, and that the location of RFP is not uniform.

The first candidate of the action to reduce this warpage is to change the core thickness to be bigger. The original design had the 300 μm core thickness. On the condition of 600 μm core, the simulation result showed that the warpage is reduced from 0.042 % to 0.029 %. Therefore, 30 % reduction is expected.

On the other hand, another candidate is to remove the unbalance of the copper remained ratio. The difference of the copper remained ratio between the outermost front side copper layer FC2 and back side copper layer BC2, which the original design has, was 35 %. According to the designer of this board, this unbalance is able to be reduced to 2 %. Therefore, the simulation is performed with 2 % delta between FC2 and BC2. The differences between FC1 and BC1, and, IP1 and IP2, were under 2 % originally. The simulation result showed 0.027 % as the warpage. Therefore, 35 % reduction is expected from the original design. After this assessment, the numerical analysis with mounting the package as the final product is applied. Then it is confirmed that the reliability level satisfies the customer needs.

The build-up board has the sandwich structure basically, and the same thickness copper and insulation layers on both front and back side. Therefore, if the copper remained ratios are equal between front and back side, and not varied depending on the horizontal location, the board is not bended by the thermo-mechanical stress. However, on the actual hardware manufacturing, it is sometimes reported that the board refuses to mount the package because the board itself has the warpage when it is manufactured. It is very important to reduce the copper unbalance between front side and back side, and also the unbalance which is depending on the horizontal location.

7. Conclusion

For the high density packaging mounting on the build-up board, the followings are suggested.

The accurate numerical analysis was established on the short analysis time, with 5 compact modeling methods.

The estimation of the connectivity reliability for the package became available with the solder plastic strain simulated by this nonlinear FEM.

The most reliable design for the CSP package was found.

The design approach for reliable FCA package was shown.

Finally the influence of the copper balance between the front side and back side copper layers is studied.

The pitch of these package solder joints is expected to get much smaller. This means that it has higher risk of decreasing the reliability of the solder connectivity. We believe the FEM model, which has been established this time, can be utilized in the development of new products.

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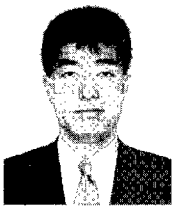

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